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Novel High-Speed QAM Receiver Architecture

Tech ID: 33909 / UC Case 2022-939-0

BRIEF DESCRIPTION

This technology introduces a revolutionary receiver architecture capable of demodulating high-order QAM signals without the need for high-speed analog-to-digital converters (ADCs), significantly enhancing communication speed and efficiency.

FULL DESCRIPTION

The invention presents a novel receiver architecture designed for ultra-high-speed communications, employing a carrier synchronization loop and a high-speed pipelined structure. This architecture uniquely demodulates high-order QAM signals directly into raw bit-streams, bypassing the need for ADCs in the signal path and addressing the critical bottleneck in conventional receiver designs.

SUGGESTED USES

» Wireless front-haul/back-haul in 5G, 6G, and beyond wireless networks.
» Coherent optical communications.
» Next-generation wireline systems requiring ultra-high data rates.

ADVANTAGES

» Eliminates the need for high-speed-resolution ADCs, reducing power consumption and cost.
» Supports demodulation of any 4N-QAM signal at arbitrary carrier frequencies.
» Improves communication speed by removing the ADC bottleneck.

PATENT STATUS

Country	Type	Number	Dated	Case
Patent Cooperation Treaty	Published Application	WO 2024/020140	01/25/2024	2022-939

Additional Patent Pending

RELATED MATERIALS

» Oveisi, M., Wang, H., Heydari, P. (2023). A Study of a Millimeter-Wave Transmitter Architecture Realizing QAM Directly in RF Domain. IEEE Transactions on Circuts and Systems I: Regular Papers, 70 (6).

CONTACT

Edward Hsieh
hsiehe5@uci.edu
tel: 949-824-8428.

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