Integrated Dielectric Waveguide and Semiconductor Layer

Tech ID: 22906 / UC Case 2013-142-0

BRIEF DESCRIPTION

A new technique for integrating ultra-low loss waveguides (ULLWs) with active silicon and/or compound semiconductor waveguides on a common substrate.

BACKGROUND

Silicon photonics and its integration with well-known CMOS fabrication technology have the potential to solve inevitable speed bottlenecks in future computing and chip platforms. UCSB's iPHOD group has developed a unique approach to create ultra-low loss waveguides (ULLWs) using extremely thin silicon nitride cores and thermally grown SiO2 layers, resulting in waveguides with low confinement, low effective index and ultra-low loss values below 0.1 dB/m. Current approaches to integrate these ULLW layers with active photonics layers (where silica waveguides are deposited on top of an active silicon layer) are not possible because the fabrication technology proposed is not directly compatible with ULLW technology, due to the limited thickness of the lower cladding area and its inability to withstand the high heat of the ULLW process.

DESCRIPTION

Researchers at the University of California, Santa Barbara have discovered a new technique for integrating ultra-low loss waveguides (ULLWs) with active silicon and/or compound semiconductor waveguides on a common substrate. By adding the silicon photonic layer through a back-end process, this new approach guarantees thermal-budget, stress-budget, and lower cladding thickness compatibility, and preserves the single-crystalline nature and tight thickness tolerance of a silicon-on-insulator (SOI) waveguide layer. This technique is important for producing high-quality silicon devices and further integrating III-V materials on top of silicon layers. This technique is also well suited for applications such as optical telecommunications and data communications.

ADVANTAGES

- Preserves performance of ULLWs (< 0.1 dB/m) and active silicon layers
- Same tight thickness tolerance of SOI waveguide layer
- Increased bandwidth due to tapered couplers
- Decreased overall costs

APPLICATIONS

- Silicon photonics

CONTACT

Pasquale S. Ferrari
ferrari@tia.ucsb.edu
tel: .

INVENTORS

- Bauters, Jared
- Blumenthal, Daniel J.
- Bovington, Jock T.
- Bowers, John E.
- Davenport, Michael
- Heck, Martijn

OTHER INFORMATION

KEYWORDS

waveguides, photonics, silicon, cenIEE, indtelecom, indmicroelec

CATEGORIZED AS

- **Optics and Photonics**
  - All Optics and Photonics
- **Semiconductors**
  - Materials

RELATED CASES

2013-142-0

- Optical telecommunications and data communications

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,285,540	03/15/2016	2013-142

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Bonding of Heterogeneous Material for Improved Yield and Performance of Photonic Integrated Circuits
- Epitaxial Laser Integration on Silicon Based Substrates
- A Hybrid Silicon Laser-Quantum Well Intermixing Wafer Bonded Integration Platform
- Integrated Reconfigurable Circulator
- Magneto-Optic Modulator
- Quantum Dot Photonic Integrated Circuits
- Ring Resonator-Based Optical Isolator and Circulator
- Orthogonal Mode Laser Gyro
- Loss Modulated Silicon Evanescent Lasers
- Monolithically Integrated Laser-Nonlinear Photonic Devices
- Misfit Dislocation Free Quantum Dot Lasers

University of California, Santa Barbara
Office of Technology & Industry Alliances
342 Lagoon Road, ,Santa Barbara,CA 93106-2055 |
www.tia.ucsb.edu
Tel: 805-893-2073 | Fax: 805.893.5236 | padilla@tia.ucsb.edu