Methods for Integrated Circuit C4 Ball Placement Considering Package Reliability

Tech ID: 21670 / UC Case 2011-244-0

BACKGROUND

Due to the growing complexity and size of integrated circuits (ICs), the importance of the I/O requirements continues to grow. Moreover, the large I/O count found on most ICs has forced designers to use flip-chip packaging instead of wire bonded packaging. The flip-chip approach uses Controlled Collapse Chip Connections, also known as C4 to increase electrical contact density. Electromigration is the transport of material by conductor ions due to momentum transfer between conducting electrons and metal atoms. Unfortunately, the C4 solder bumps in flip-chip packaging are susceptible to failure mechanisms such as thermal cycling and electromigration, especially in the presence of high temperatures. As C4 balls get smaller, the electron current densities in the C4 balls increase. Thus, metal transport from the C4 balls also increases. High temperature and large temperature gradients exacerbates the failure rate of modern ICs. UC Santa Cruz researchers have developed two universal methods for combating C4 failure, specifically at the CAD level.

TECHNOLOGY DESCRIPTION

UC Santa Cruz researchers have developed an algorithm which increase the life-span of integrated circuits (IC's). The revolutionary new algorithm optimizes reliability floor planning on C4 balls. By using UCSC's quadric pin placement algorithm, the C4 ball (solder balls) life expectancy improves by a record 49 times on average compared to competitors. The algorithm targets placement of data I/O C4 balls to reduce failure rate from thermal-cycle fatigue by minimizing wire-length and increasing the number of cycles to failure.

APPLICATIONS

- Modern electronic devices
- Very large scale integrated (VLSI) chips and other semiconductor devices and support elements such as resistors, inductors, capacitors and connectors

ADVANTAGES

- Improves C4 (solder balls) life expectancy by 49X

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	8,966,427	02/24/2015	2011-244

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OTHER INFORMATION

KEYWORDS

very large scale integrated chips, VLSI chips, Controlled Collapse Chip Connections, C4, solder balls, semiconductors, resistors, inductors, capacitors, connectors, I/O, integrated circuits

CATEGORIZED AS

- **Computer**
  - Other
- **Semiconductors**
  - Assembly and Packaging
  - Other

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