

Erasure-Flip Logic Gate for Momentum Computing

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ABSTRACT

Researchers at the University of California, Davis have developed a method and device performing simultaneous flip and merge operations to improve logical operation performance in high-efficiency superconducting circuits.

FULL DESCRIPTION

This technology introduces a method and apparatus that initialize circuits to an initial logical state and perform simultaneous flip and merge operations on sets of logical states to map to a final logical state, enabling more efficient and accurate logical operations. The design leverages conventional Josephson junction circuit elements and uses novel control methods thereon to synchronize these operations, leading to improved computation speed, greatly reduced energy requirements, and reliability beyond traditional quantum flux parametron approaches. The operation relies only on Josephson junction nonlinearity, which is a classical physics phenomenon and not a quantum-mechanical phenomenon.

APPLICATIONS

- ▶ High-performance, energy-efficient classical computing hardware.
- ▶ Advanced logic circuit design for next-generation, low-power processors.
- ▶ Military and defense applications requiring high-performance computation.
- ▶ Research institutions developing scalable and thermodynamically efficient logic systems.
- ▶ Computational platforms focused on reducing energy consumption and heat dissipation.

FEATURES/BENEFITS

- ▶ Increases computational efficiency by executing flip and merge operations simultaneously.
- ▶ Improves accuracy in logic operations through enhanced mapping of initial to final logical states.
- ▶ Facilitates coordinated control and operation with inductive coupling of circuit elements.
- ▶ Reduces thermodynamic inefficiencies compared to conventional quantum flux parametron technologies.
- ▶ Accelerates processing speeds by combining logical state manipulations.
- ▶ Overcomes speed, accuracy, and efficiency trade-offs in current quantum flux parametron computing.
- ▶ Addresses physical constraints and heat dissipation challenges found in CMOS-based computing.
- ▶ Mitigates inaccuracies and slowness present in existing quantum computing circuits.
- ▶ Leverages standard semiconductor fabrication technology to ensure scalability and cost-effective production.

CONTACT

Andrew M. Van Court
amvancourt@ucdavis.edu
 tel: .



INVENTORS

- ▶ Crutchfield, James P.
- ▶ Ray, Kyle J.
- ▶ Tang, Kuen Wai

OTHER INFORMATION

KEYWORDS

circuit, computation, flip operation, inductive coupling, logical operations, merge operation, quantum flux parametron, thermodynamic efficiency

CATEGORIZED AS

- ▶ **Computer**
- ▶ Hardware
- ▶ **Security and Defense**
- ▶ Other

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PATENT STATUS

Patent Pending

University of California, Davis

Technology Transfer Office

1 Shields Avenue, Mrak Hall 4th Floor,
Davis, CA 95616

Tel:

530.754.8649

techtransfer@ucdavis.edu

<https://research.ucdavis.edu/technology-transfer/>

Fax:

530.754.7620

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