Ai-Assisted Intelligent Method For Analyzing Multi-Tiered Chiplets

Tech ID: 34188 / UC Case 2024-99P-0

BRIEF DESCRIPTION

An innovative, AI-driven approach for non-intrusive analysis and defect detection in multi-tiered chiplets, enhancing microelectronics packaging.

FULL DESCRIPTION

This technology introduces an automated, AI-assisted vision method for the analysis of multi-tiered chiplets, focusing on identifying structural defects or voids without the need for invasive procedures. It leverages advanced machine learning models to convert temperature maps into detailed three-dimensional defect maps, offering a comprehensive insight into the structural integrity of microelectronics. This method is particularly crucial in the context of 3D stacking in microsystems, where seamless bonding is essential for device functionality.

SUGGESTED USES

· Quality control and assurance in semiconductor manufacturing.

· Advanced electronics packaging, particularly for 3D stacked microelectronics.

· Defect analysis and prevention in microsystem development.

· Research and development in microelectronics and materials science

ADVANTAGES

· Speed: Offers rapid measurements compared to traditional methods, providing rich features.

· Simplicity: Eliminates the need for a medium, such as water, thus avoiding potential sample damage and reducing processing time.

· Efficiency: Enhances defect detection, improving yield rates and leading to cost savings in semiconductor manufacturing.

· Intelligence: Utilizes machine learning to predict defects, understanding the link between manufacturing processes and defect evolution.

PATENT STATUS

Patent Pending

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OTHER INFORMATION

CATEGORIZED AS

» **Imaging**
» 3D/Immersive
» **Materials & Chemicals**
» Electronics Packaging
» **Sensors & Instrumentation**
» Analytical
» Process Control
» Scientific/Research
» **Engineering**
» Robotics and Automation

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