Error-Triggered Learning For Efficient Memristive Neuromorphic Hardware

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BRIEF DESCRIPTION

An innovative learning algorithm that enables efficient online training of spiking neural networks on memristive neuromorphic hardware.

FULL DESCRIPTION

This technology introduces a local, gradient-based, error-triggered learning algorithm with online ternary weight updates for multilayer Spiking Neural Networks (SNNs). It leverages memristive neuromorphic hardware for efficient computation, significantly reducing energy consumption while maintaining high performance levels. The algorithm is complemented by a hardware architecture designed for low-power operation, incorporating memristive crossbar arrays and peripheral circuitry optimized for online training in neuromorphic systems.

SUGGESTED USES

- Development of energy-efficient neuromorphic chips for AI applications.
- Advancements in lifelong learning systems for robotics and autonomous machines.
- Enhancements in edge computing devices, reducing reliance on cloud-based computations.
- Innovations in low-power, high-performance computing for wearable technology and IoT devices.
- Applications in real-time data processing and decision-making systems requiring minimal energy consumption

ADVANTAGES

- Enables online training directly on neuromorphic hardware, eliminating the need for off-chip learning.
- Significantly more energy-efficient than traditional methods, with over 80x energy improvement observed.
- Designed for low-power operation using subthreshold regime technology in a standard 180 nm CMOS process.
- Supports lifelong learning capabilities through efficient implementation of learning dynamics as synaptic plasticity.
- Addresses the von-Neumann bottleneck by reducing data shuttling between memory and processing units.

PATENT STATUS

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OTHER INFORMATION

KEYWORDS

error-triggered learning, efficient training, neuromorphic chip, AI accelerator

CATEGORIZED AS

- **Computer**
  - Hardware

RELATED CASES

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Country	Type	Number	Dated	Case
United States Of America	Published Application	2022109593	05/25/2022	2021-744

RELATED MATERIALS

» Payvand, Melika, et al. "On-chip error-triggered learning of multi-layer memristive spiking neural networks." IEEE Journal on Emerging and Selected Topics in Circuits and Systems 10.4 (2020): 522-535.

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