

# MEMORY CELLS USING NEGATIVE DIFFERENTIAL RESISTANCE FERROELECTRIC FETS

Tech ID: 33563 / UC Case 2024-135-0

## PATENT STATUS

Country	Type	Number	Dated	Case
Patent Cooperation Treaty	Published Application	WO 2025/245395	11/27/2025	2024-135

## BRIEF DESCRIPTION

As the demand for higher memory density in modern computing continues to grow, traditional static memory architectures face physical scaling limits. To address this, UC Berkeley researchers have developed a novel static memory bit-cell that utilizes negative differential resistance (NDR) ferroelectric field-effect transistor (FeFET) devices. By exploiting the specific NDR characteristics inherent in these FeFETs, a stable binary data latch can be formed using as few as two devices, providing a path toward significantly more compact storage than standard SRAM cells. The design further incorporates a transfer FET to manage reading and writing functions, offering a streamlined circuit that reduces complexity while maintaining high performance.

## SUGGESTED USES

- » High-Density SRAM: Replacement for traditional six-transistor (6T) SRAM cells in high-performance processors to increase on-chip cache capacity.
- » Low-Power Embedded Systems: Implementation in IoT devices where compact memory footprints and low energy consumption are critical for battery life.
- » Mobile Computing: Integration into mobile system-on-chips (SoCs) to allow for more memory in smaller form factors.
- » Edge AI Hardware: Serving as high-efficiency local storage for artificial intelligence accelerators that require rapid data access and high density.
- » Space-Constrained Electronics: Use in wearable technology and medical implants where physical space for silicon components is extremely limited.

## ADVANTAGES

- » Superior Compactness: Utilizes significantly fewer transistors than traditional memory cells, allowing for a much higher density of memory on a single die.
- » Simplified Circuitry: The use of only two devices for a binary latch reduces the number of interconnects and potential points of failure.
- » High Efficiency: Exploiting NDR characteristics allows for stable data retention with reduced power overhead compared to conventional static memory designs.
- » FeFET Integration: Leverages the unique properties of ferroelectric materials, which can offer improved switching speeds and non-volatile potential.

## CONTACT

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## INVENTORS

- » Tatum, Lars Prospero

## OTHER INFORMATION

### CATEGORIZED AS

- » Computer
  - » Hardware
  - » Nanotechnology
    - » Semiconductors
      - » Design and Fabrication

### RELATED CASES

2024-135-0

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Scalable Design: The architecture is compatible with single or dual transfer FET configurations, providing flexibility for different reading and writing speed requirements.

## RELATED MATERIALS

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### ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

► [NDR Ferroelectric FET and Method of Operating the Same](#)



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