DYNAMIC READ FEFET MEMORY

Tech ID: 33390 / UC Case 2024-070-0

PATENT STATUS

Country	Type	Number	Dated	Case
Patent Cooperation Treaty	Published Application	WO 2025/166219	08/07/2025	2024-070

Additional Patent Pending

BRIEF DESCRIPTION

Researchers at UC Berkeley have designed a novel Dynamic Read Access Ferroelectric Memory (DyRAFeM) device that addresses the scalability limitations of conventional flash memory. The architecture features a substrate with a semiconductor channel positioned between a source and a drain, topped by a sophisticated gate stack. Unlike traditional ferroelectric field-effect transistors (FEFETs), this design integrates a metal layer forming a floating gate directly between the gate oxide and the ferroelectric layer. This specific configuration enables robust non-volatile memory functionality while allowing for significantly improved scaling. By optimizing the interaction between the floating metal gate and the ferroelectric material, the device provides a path toward higher-density, high-speed memory arrays suitable for the next generation of microelectronics.

SUGGESTED USES

- High-Density Non-Volatile Memory: Replacing or augmenting traditional NAND/NOR flash in mobile devices and solid-state drives.
- Edge Computing: Providing fast, low-power storage for IoT devices that require frequent data logging and non-volatile retention.
- Embedded Systems: Integrating scalable memory directly into microcontrollers for automotive and industrial applications.
- Artificial Intelligence Accelerators: Supporting on-chip weight storage for neural networks where high-speed read access and high density are critical.
- Data Centers: Enhancing the performance of storage class memory (SCM) to bridge the gap between DRAM and traditional long-term storage.

ADVANTAGES

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INVENTORS

- Salahuddin, Sayeef

OTHER INFORMATION

CATEGORIZED AS

- **Computer**
  - Hardware
- **Research Tools**
  - Other
- **Semiconductors**
  - Design and Fabrication
  - Materials

RELATED CASES

2024-070-0

Superior Scalability: The unique gate stack architecture allows the memory cells to be scaled down further than conventional flash technology without loss of performance.

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Non-Volatile Functionality: Retains stored data without power, combining the benefits of dynamic access with long-term retention.

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Enhanced Read Dynamics: The DyRAFeM design is optimized for high-speed read operations, improving overall system latency.

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Improved Device Stability: The inclusion of a metal floating gate helps manage the electric field distribution across the ferroelectric layer, leading to more reliable switching.

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CMOS Compatibility: The materials and structure are designed to be compatible with standard semiconductor fabrication processes.

RELATED MATERIALS

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Superlattice, Ferroic Order Thin Films For Use As High/Negative-K Dielectric
- Giant Energy And Power Density Microcapacitors Via Ferroic Order Superlattices

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