DESIGN WORKFLOW IMPROVEMENTS USING STRUCTURAL MATCHING FOR FAST RE-SYNTHESIS OF ELECTRONIC CIRCUITS

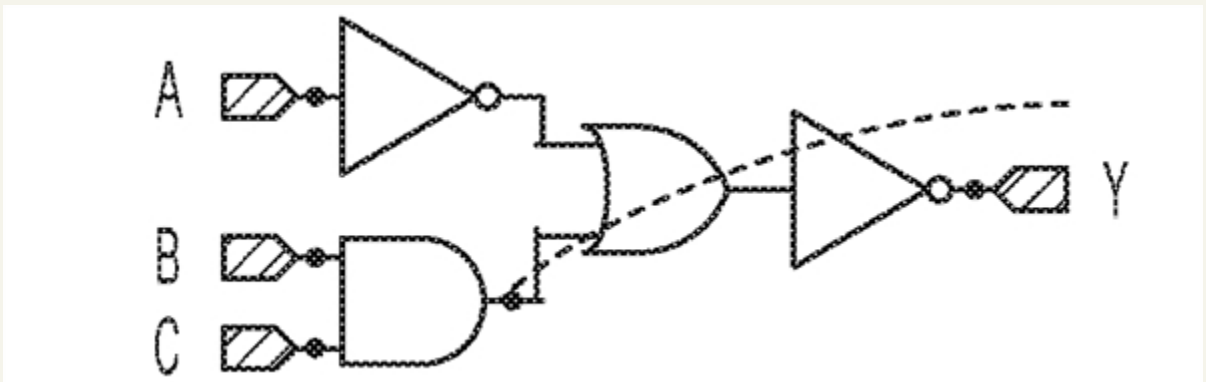
Tech ID: 32773 / UC Case 2018-689-0

BACKGROUND

Electronic circuits are growing in complexity every year. Existing workflows that optimize the design and placement of circuit components are laborious and time-consuming though. Incremental design changes that target device optimization can take many hours to render. Streamlined design workflows that are both fast and able to optimize performance are needed to keep pace with these device improvements. A UC Santa Cruz researcher has developed a new technique, SMatch, to shorten design workflow times with minimal QoR impact.

TECHNOLOGY DESCRIPTION

UC Santa Cruz researchers have developed SMatch, a method that uses an incremental FPGA flow to skip placement and routing for matching blocks. This method significantly shortens runtime while maintaining QoR by reducing the overall number of LUTs needed to be placed and routed. SMatch is generally 20x faster than other incremental commercial FPGA flows and is able to deliver many of the changes set by the Anubis benchmark suite in under 30s.



APPLICATIONS

- Electronic design automation workflow for commercial use

ADVANTAGES

- 16 to 20x faster synthesis, placement, and routing than current state-of-the-art flow, LiveSynth
- Comparable QoR

INTELLECTUAL PROPERTY INFORMATION

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	11,599,700	03/07/2023	2018-689

CONTACT

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OTHER INFORMATION

KEYWORDS

Electronic device automation, EDA, Design workflow, Synthesis, Chip design, Structural Netlist, FPGA - Field Programmable Gate Array, Hardware Description Language, Lookup Table

CATEGORIZED AS

- Computer
- Hardware
- Software

RELATED CASES

2018-689-0

United States Of America	Issued Patent	10,885,246	01/05/2021	2018-689	

RELATED MATERIALS

- SMatch: Structural Matching for Fast Resynthesis in FPGAs - 06/02/2019

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Livesynthesis: Towards An Interactive Synthesis Flow

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