(SD2020-249) Adaptive Bias Circuits For CMOS Millimeter-Wave Power Amplifiers: state-of-the-art back-off efficiency for silicon Ka-band Doherty PAs using single inputs and without digital predistortion

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BACKGROUND

Power amplifier performance for emerging 5G mm-wave systems poses significant challenges for output power, efficiency and linearity. Efficiency in backoff is a key concern, given the peak-to-average power ratio of order 6-9dB for 5G signals. As a result, considerable attention has been given to composite amplifiers featuring backoff efficiency enhancement, particularly Doherty amplifiers.

Adaptive bias circuits have been previously developed for use with power amplifiers at low microwave frequencies (for example, 1-2GHz as applied in 2G, 3G and 4G cellular networks). Direct application of these techniques is not straightforward at higher frequencies, such as 28GHz as used for 5G wireless communications, because the transistors have less gain at the high frequencies.

TECHNOLOGY DESCRIPTION

Researchers from UC San Diego have designed a family of adaptive bias circuits that are straightforward to incorporate in the amplifier, and do not load down the input and decrease the amplifier gain. The adaptive bias circuits boost gate bias voltage when the input power gets to be high. This power applifier technology provides state-of-the-art back-off efficiency for silicon Ka-band Doherty PAs using single inputs and without digital predistortion, while providing high gain and output power.

APPLICATIONS

The adaptive bias circuits are of major interest for mm-wave transmitters employing antenna arrays and using modulated output signals that require high linearity. In such systems, it is generally not cost effective to provide digital predistortion capability for each power amplifier – thus the power amplifier must be linear on its own. The linearity improvement provided with the adaptive bias circuits described here is a significant benefit. It allows operation without the large backoff power levels needed with conventional amplifiers while still maintaining required system linearity, and thus can provide higher power and efficiency for the system. Systems that can directly benefit are 5G wireless communication systems, satellite communication systems, several military communication systems and advanced radar systems that use complex modulations.

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OTHER INFORMATION

KEYWORDS

5G mobile communication, Wireless communication, Impedance matching, Power amplifiers, Power generation, MOS devices, silicon-on-insulator, microwave power amplifiers, integrated circuit design, CMOS integrated circuits, mm-wave power amplifiers, high efficiency amplifiers, cmos-soi, 5G

CATEGORIZED AS

- **Communications**
  - Wireless
- **Energy**
  - Transmission
- **Engineering**
  - Engineering

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ADVANTAGES

The gain flatness near the maximum output power is improved (thus overcoming the “soft saturation” effect that shows up in many CMOS PAs). The phase of the output can also be kept more constant at high power by using these techniques with representative FETs and amplifier configurations. An additional important benefit for mm-wave CMOS power amplifiers is that the adjustment in gate bias reduces that maximum drain to gate voltage experienced by the controlled transistor and as a result decreases the degradation process of time dependent dielectric breakdown (TDDB) that is an important limiter to the performance of mm-wave CMOS PAs. Adjustment of the reference dc voltage of the adaptive bias circuit can alter the gain and phase profiles that become degraded when the output load deviates from 50 ohms. Multiple adaptive bias circuits can be used for the different transistors of compound amplifiers. For example, in a Doherty amplifier, there are transistors (often several of them) in the main path and in the auxiliary path. The overall linearity of the Doherty amplifier can be adjusted with the use of multiple adaptive bias circuits controlling the transistor biases.

Circuit features include: 1) advanced output combiner design that achieves lower losses than conventional impedance inverter implementation; 2) adaptive biasing for linearization and backoff efficiency enhancement; 3) use of pMOS rather than nMOS to provide the potential for superior reliability; 4) compact input power splitter.

This PA provides state-of-the-art back-off efficiency for silicon Ka-band Doherty PAs using single inputs and without digital predistortion, while providing high gain and output power.

STATE OF DEVELOPMENT

In the cited paper below (Alluri et al. 2021), a Ka band Doherty amplifier is reported which achieves a combination of high power (23dBm Psat), high efficiency in backoff (29% at 6dB backoff, 24% at 8 dB backoff), high gain (16dB, stemming from a 2 stage design) and high linearity (enhanced by adaptive bias circuit linearizers) at 26 GHz in 45nm CMOS-SOI technology.

INTELLECTUAL PROPERTY INFO

This patent pending technology is available for commercial deployment. Please contact UC San Diego's Commercialization Office for licensing terms.

RELATED MATERIALS

- Alluri, S., Rostomyan, N., & Asbeck, P. (2021, January). A Ka Band 2-Stage Linear Doherty Amplifier with 23dBm Psat and 29% 6dB-Backoff PAE in pMOS-SOI. In 2021 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR) (pp. 52-54). IEEE. - 01/17/2021

PATENT STATUS

Patent Pending

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