Reducing Electrical Current Variations in Phase-Locked Loop Systems

Tech ID: 32424 / UC Case 2021-623-0

ABSTRACT

Researchers at the University of California, Davis have developed a method of eliminating electrical current mismatches in the charge pumps of phase-locked loops (PLL) systems - thereby increasing their power efficiency and phase detection capabilities.

FULL DESCRIPTION

Telecommunication systems and other signal processing applications often require frequency generation or matching. Traditional phase-frequency detector (PFD)-based phase-locked looping (PLL) is the standard technology currently for generating and synthesizing accurate frequencies. Sub Sampling Phase Locked Loop (SSPLL) technologies use a charge pump to help control the regulation of the electrical current sent into the filtering loop of the SSPLL. However, these charge pumps are highly susceptible to small voltage fluctuations that can reduce their locking range and lead to large output signal distortions. A method of regulating charge pump current would allow for the creation of a much more efficient SSPLL design – resulting in a better locking range, improved gain, and reduced power consumption.

Researchers at the University of California Davis have developed a method of compensating for mismatched current in charge pumps. This new, SSPLL technology includes a sub-sampling phase detector (SSPD), a charge pump, a loop filter, a voltage-controlled oscillator (VCO), and a frequency-locked loop - which ensures a desired output frequency. It also implements a charge pump current mismatch compensation structure containing a "dummy" charge pump and feedback loops. The feedback loops sense the output voltage of the charge pump and provide compensating current to both the actual charge pump and the "dummy" pump – thus eliminating the electrical current mismatch. As a result, the voltage control locking range improves from 50% of the supply voltage to 75% - enabling the SSPLL to match frequencies more quickly. The signal gain improves as well, as degeneration associated with the phase detector is eliminated. Power consumption is also reduced, as the simplified voltage control design allows the supply voltage to be as low as 0.5V. This improvement is particularly important when operating at high frequencies. This technology is a significant improvement over existing SSPLL systems, and can be implemented in a wide variety of electronic circuits.

APPLICATIONS

- Telecommunications, computer hardware, and other signal processing systems operating at high frequencies

FEATURES/BENEFITS

- An improved locking range provides for faster phase matching in SSPLL systems
- Reduced power consumption, especially at high frequencies (30-1000 GHz)
- Can be operated at under 0.5V supply voltage

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	12,155,392	11/26/2024	2021-623
Patent Cooperation Treaty	Published Application	2022/125188	07/21/2022	2021-623

CONTACT

Michael M. Mueller
mmmueller@ucdavis.edu
tel: .



INVENTORS

- Momeni, Omeed
- Wang, Hao

OTHER INFORMATION

KEYWORDS

Phase-locked loop, sub-sampling phase-locked loop, SSPLL, analog circuit, electrical current mismatch

CATEGORIZED AS

- **Communications**
  - Other
- **Computer**
  - Hardware
  - Other
- **Sensors & Instrumentation**
  - Other
  - Process Control

RELATED CASES

2021-623-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Reversed Feedback Amplifier Architecture
- Ultra-High Range Resolution Doppler Radar Front End With Quadrature-Less Coherent Demodulation
- Field Effect Bipolar Transistor
- Low Energy and Noise Sub-Sampling Phase-Locked Loop
- High-Frequency Imaging and Data Transmission Using a Re-configurable Array Source with Directive Beam Steering
- Hybrid Electromechanical Metamaterials for Optical and Electrical Devices
- Phased-Locked Loop Coupled Array for Phased Array Applications

- Scalable Phased Array Standing Wave Architecture
- Embedded Power Amplifier

University of California, Davis
Technology Transfer Office
1 Shields Avenue, Mrak Hall 4th Floor,
Davis,CA 95616

Tel: 530.754.8649
techtransfer@ucdavis.edu
https://research.ucdavis.edu/technology-transfer/
Fax: 530.754.7620

© 2021 - 2024, The Regents of the University of California
Terms of use
Privacy Notice