N-polar III-N Semiconductor Device Structures Enabled by Wet Chemistry
Tech ID: 31967 / UC Case 2020-703-0

BACKGROUND

Current techniques for fabricating GaN-based semiconductor devices rely on the use of dry etch processes that use plasmas generated from gaseous species to remove III-N layers. Consequently, the nature of the plasma generated for dry etch processes is known to result in both surface and subsurface damage from exposure to high-energy charged ions and electrons. Due to the chemical stability of metal-polar surfaces, dry etching is the only viable approach to etch metal-polar surfaces. Additionally, these metal-polar devices have demonstrated limited RF capabilities relative to N-polar transistors fabricated by dry etch techniques. Thus, overcoming dry etching limitations would allow for drastic improvement of N-polar III-N device performance while also reducing manufacturing costs.

DESCRIPTION

Researchers at the University of California, Santa Barbara have developed wet etch processes that can be used to fabricate N-polar III-N transistors to reduce trapping effects, lower leakages, lower noise, and increase reliability. N-polar surfaces are more reactive relative to metal-polar surfaces enabling this technique. Furthermore, N-polar GaN transistors demonstrate superior RF performance, particularly at mm-wave frequencies relative to metal-polar transistors. In addition to lowering capital costs as a result of a simplified infrastructure, wet etching also reduces manufacturing cost with batch processing that can scale between different substrate sizes more easily than with dry etching. Therefore, this invention allows for the fabrication of higher performance devices in a simplified and cost-efficient manner.

ADVANTAGES

▶ Improves device performance
▶ Reduces costs
▶ Commercially scalable

APPLICATIONS

▶ III-N Devices
▶ GaN Transistors

PATENT STATUS

Patent Pending

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

▶ Achieving “Active P-Type Layer/Layers” In III-Nitride Epitaxial Or Device Structures Having Buried P-Type Layers
▶ High-Quality N-Face GaN, InN, AlN by MOCVD
▶ Defect Reduction in GaN films using in-situ SiNx Nanomask
▶ Device Structures Utilizing Barrier Enhancement Conductive Materials on N-polar III-N
▶ Laser Diode With Tunnel Junction Contact Surface Grating
▶ High Mobility Group-III Nitride Transistors with Strained Channels
▶ A Structure For Increasing Mobility In A High-Electron-Mobility Transistor
▶ Fabrication of Relaxed Semiconductor Films without Crystal Defects
▶ Improved Fabrication of Nonpolar InGaN Thin Films, Heterostructures, and Devices
Methods for Locally Changing the Electric Field Distribution in Electron Devices

Controlling Linearity in N-Polar GaN MISHEMTs

Technique for the Nitride Growth of Semipolar Thin Films, Heterostructures, and Semiconductor Devices

Enabling Epitaxial Growth On Thin Substrates

(In,Ga,Al)N Optoelectronic Devices with Thicker Active Layers for Improved Performance

GaN-based Vertical Metal Oxide Semiconductor and Junction Field Effect Transistors

Novel Current-Blocking Layer in High-Power Current Aperture Vertical Electron Transistors (CAVEtS)

III-N Transistor With Stepped Cap Layers

Polarization-Doped Field Effect Transistors with Increased Performance

Wafer Bonding for Embedding Active Regions with Relaxed Nanofeatures

III-N Based Material Structures and Circuit Modules Based on Strain Management