Low Energy and Noise Sub-Sampling Phase-Locked Loop

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ABSTRACT

Phase locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency, or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Researchers at the University of California, Davis have invented a novel, sub-sampling phase-locked, loop (SSPLL) that uses a sub-sampling lock detector (SSLD) to monitor the harmonic selected by the SSPLL. This technology requires lower energy consumption and reduces signal noise.

FULL DESCRIPTION

Phase-Locked Loops (PLL) couple the output signal with the input signal, which creates a relationship between their phases. Such loops promote synchronization and assist in extracting the information carried by frequency-modulated signals. While traditional PLLs use frequency dividers, this approach can generate significant signal noise. Thus, sub-sampling phase-locked loops (SSPLLs) are usually preferred – as they produce lower in-band phase noise. However, SSPLLs require a frequency locked loop (FLL) to avoid locking to the wrong harmonic input of the input frequency. The FLLs used require a large amount of energy when the input is a millimeter wave. This reality often leaves the user forced to choose between either having a noisy signal or consuming significant power.

Researchers at the University of California, Davis have invented a SSPLL that uses a sub-sampling lock detector (SSLD) to monitor the harmonic selected by the SSPLL. The SSLD together with an on-chip generated, high frequency reference can automatically detect if the SSPLL has locked onto the wrong frequency. Then, the SSPLL can correct to the proper harmonic. Since the SSLD and high frequency reference generation circuits contain no millimeter wave frequency dividers, they consume much less power than a traditional FLL. Hence, this invention allows for a millimeter wave SSPLL that is simultaneously low-noise and low-power.

APPLICATIONS

- Phase-Locked Loop for generating an output signal with phase related to the input signal

FEATURES/BENEFITS

- Able to be used for millimeter wave signals
- Sub-sampling generates a low-noise signal
- Monitoring system for SSLD is low-power

PATENT STATUS

Country	Type	Number	Dated	Case

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OTHER INFORMATION

KEYWORDS

Phase Locked Loop, Frequency Divider, Lock Detector, Signal Coupling

CATEGORIZED AS

- **Computer**
  - Hardware
- **Semiconductors**
  - Design and Fabrication
- **Engineering**
  - Other

RELATED CASES

2019-553-0

United States Of America	Issued Patent	10,992,303	04/27/2021	2019-553

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Reversed Feedback Amplifier Architecture
- Ultra-High Range Resolution Doppler Radar Front End With Quadrature-Less Coherent Demodulation
- Field Effect Bipolar Transistor
- High-Frequency Imaging and Data Transmission Using a Re-configurable Array Source with Directive Beam Steering
- Hybrid Electromechanical Metamaterials for Optical and Electrical Devices
- Phased-Locked Loop Coupled Array for Phased Array Applications
- Scalable Phased Array Standing Wave Architecture
- Embedded Power Amplifier
- Reducing Electrical Current Variations in Phase-Locked Loop Systems

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