Iii-N Transistor With Stepped Cap Layers
Tech ID: 30302 / UC Case 2019-418-0

BRIEF DESCRIPTION
A new structure for III-N transistors that is able to maintain a high breakdown and operating voltage while improving the gain of the device.

BACKGROUND
Traditional N-polar GaN deep recess HEMTs that are used for power amplification at mm-wave frequencies offer a high power density that is 4x larger than traditional Ga-polar HEMT structures. However, it is significantly smaller than the 40 W/mm of output power that has been demonstrated by other devices that use field plates. While field plates are known to increase voltage, they also require additional capacitances that ultimately limit the gain of the transistor making them less optimal. A structure that maximizes voltage while maintaining gain would significantly improve current transistors.

DESCRIPTION
Researchers at the University of California, Santa Barbara have created a new structure for III-N transistors that is able to maintain a high breakdown and operating voltage while improving the gain of the device. A stepped cap design is used to increase the operating voltage of the transistor and therefore provides a higher output power. Additionally, having a device that offers higher power allows for greatly simplified system level design due to the need for fewer parts to be combined.

ADVANTAGES
▶ Increased breakdown voltage
▶ More reliable device operation
▶ Increased power allows for a simplified system with fewer parts

APPLICATIONS
▶ GaN-Based Transistors
▶ Solid State Lighting

PATENT STATUS
Patent Pending

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS
▶ Achieving “Active P-Type Layer/Layers” In III-Nitride Epitaxial Or Device Structures Having Buried P-Type Layers
▶ High-Quality N-Face GaN, InN, AlN by MOCVD
▶ Defect Reduction in GaN films using in-situ SiNx Nanomask
▶ Device Structures Utilizing Barrier Enhancement Conductive Materials on N-polar III-N
▶ Laser Diode With Tunnel Junction Contact Surface Grating
▶ High Mobility Group-III Nitride Transistors with Strained Channels
▶ A Structure For Increasing Mobility In A High-Electron-Mobility Transistor
▶ Fabrication of Relaxed Semiconductor Films without Crystal Defects
▶ Improved Fabrication of Nonpolar InGaN Thin Films, Heterostructures, and Devices
▶ Methods for Locally Changing the Electric Field Distribution in Electron Devices
▶ Near-Infrared, Flip-Chip, TCO-Clad, InGaN Quantum Dot Laser Diode
Incorporating Temperature-Sensitive Layers in III-N Devices

Controlling Linearity in N-Polar GaN MISHEMTs

Technique for the Nitride Growth of Semipolar Thin Films, Heterostructures, and Semiconductor Devices

Enabling Epitaxial Growth On Thin Substrates

(In,Ga,Al)N Optoelectronic Devices with Thicker Active Layers for Improved Performance

N-polar III-N Semiconductor Device Structures Enabled by Wet Chemistry

GaN-based Vertical Metal Oxide Semiconductor and Junction Field Effect Transistors

Novel Current-Blocking Layer in High-Power Current Aperture Vertical Electron Transistors (CAVETs)

Polarization-Doped Field Effect Transistors with Increased Performance

Wafer Bonding for Embedding Active Regions with Relaxed Nanostructures

III-N Based Material Structures and Circuit Modules Based on Strain Management