Iii-N Transistor With Stepped Cap Layers

Tech ID: 30302 / UC Case 2019-418-0

BRIEF DESCRIPTION

A new structure for III-N transistors that is able to maintain a high breakdown and operating voltage while improving the gain of the device.

BACKGROUND

Traditional N-polar GaN deep recess HEMTs that are used for power amplication at mm-wave frequencies offer a high power density that is 4x larger than traditional Ga-polar HEMT structures. However, it is significantly smaller than the 40 W/mm of output power that has been demonstrated by other devices that use field plates. While field plates are known to increase voltage, they also require additional capacitances that ultimately limit the gain of the transistor making them less optimal. A structure that maximizes voltage while maintaining gain would significantly improve current transistors.

DESCRIPTION

Researchers at the University of California, Santa Barbara have created a new structure for III-N transistors that is able to maintain a high breakdown and operating voltage while improving the gain of the device. A stepped cap design is used to increase the operating voltage of the transistor and therefore provides a higher output power. Additionally, having a device that offers higher power allows for greatly simplified system level design due to the need for fewer parts to be combined.

ADVANTAGES

- Increased breakdown voltage
- More reliable device operation
- Increased power allows for a simplified system with fewer parts

APPLICATIONS

- GaN-Based Transistors
- Solid State Lighting

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	11,594,625	02/28/2023	2019-418

CONTACT

Pasquale S. Ferrari
ferrari@tia.ucsb.edu
tel: .

INVENTORS

- Guidry, Matthew
- Keller, Stacia
- Mishra, Umesh K.
- Romanczyk, Brian R.
- Zheng, Xun

OTHER INFORMATION

KEYWORDS

indefeat, indled, LED, Light-Emitting Diode, Semiconductors, GaN-Based Transistors, Solid State Lighting, III-N Transistor Structure, Gallium Nitride (GaN), Stepped Cap Layers

CATEGORIZED AS

- **Energy**
  - Lighting
- **Materials & Chemicals**
  - Other
- **Semiconductors**
  - Other

RELATED CASES

2019-418-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- High-Quality N-Face GaN, InN, AlN by MOCVD
- Defect Reduction in GaN films using in-situ SiNx Nanomask
- A Structure For Increasing Mobility In A High-Electron-Mobility Transistor
- Improved Fabrication of Nonpolar InGaN Thin Films, Heterostructures, and Devices
- Methods for Locally Changing the Electric Field Distribution in Electron Devices
- Technique for the Nitride Growth of Semipolar Thin Films, Heterostructures, and Semiconductor Devices
- (In,Ga,Al)N Optoelectronic Devices with Thicker Active Layers for Improved Performance
- GaN-based Vertical Metal Oxide Semiconductor and Junction Field Effect Transistors
- Novel Current-Blocking Layer in High-Power Current Aperture Vertical Electron Transistors (CAVETs)
- III-N Based Material Structures and Circuit Modules Based on Strain Management

University of California, Santa Barbara
Office of Technology & Industry Alliances
342 Lagoon Road, ,Santa Barbara,CA 93106-2055 |
www.tia.ucsb.edu
Tel: 805-893-2073 | Fax: 805.893.5236 | padilla@tia.ucsb.edu