Selective Deposition Of Diamond In Thermal Vias

Tech ID: 30129 / UC Case 2015-453-0

SUMMARY

UCLA researchers in the Department of Materials Science & Engineering have developed a new method of diamond deposition in integrated circuit vias for thermal dissipation.

BACKGROUND

Modern integrated circuits (IC) are typically fabricated by growing layers of semiconductors on a substrate. This growing method, epitaxial fabrication, has enabled tighter packing of chip components and the implementation of complex circuits. These advancements have allowed higher-frequency chips reaching the GHz range. However, as chips become more crowded and complex, heat dissipation becomes an issue. Raised temperatures may not only reduce component performance, but its lifetime and reliability as well. Due to the desirable thermal and electrical properties of diamond, it has been proposed for coating the inner surfaces of vias (conducting paths between IC layers) to transfer heat from conductors to the substrate. However, both large and small vias require selective coating methods to avoid wafer bowing and breakage. A reliable method to coat vias with diamond can drastically boost the performance of densely packed integrated circuits.

INNOVATION

UCLA researchers have developed a novel fabrication method that enables selective deposition of diamonds in thermal IC vias. A key point of innovation is this method's selectivity, allowing manufacturers to tailor deposition properties based on the size of a via. Additionally, diamond deposition only occurs within the via, eliminating wasted diamond on planar surfaces that would need to be removed afterward. This method ultimately enables higher-performing IC's while minimizing mechanical defects such as bowing and breakage due to thermal coefficient mismatches as well as wasted bulk material.

APPLICATIONS

- IC design and manufacturing
- High power applications
- Miniature systems such as handheld devices and autonomous systems

ADVANTAGES

- Selective process enables targeting of small or large vias
- Avoids undesirable IC mechanical bending and breaking
- Efficient and targeted process with minimal bulk material wastage

PATENT STATUS

Country	Type	Number	Dated	Case
Japan	Issued Patent	6345247	06/01/2018	2015-453
Taiwan	Issued Patent	I552193	10/01/2016	2015-453
United States Of America	Issued Patent	9,196,703	11/24/2015	2015-453
Republic Of Korea (South Korea)	Published Application	10-2015-0044489	04/25/2016	2015-453

Additional Patent Pending

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OTHER INFORMATION

KEYWORDS

diamond, via, conductor, conducting, substrate, thermal, interconnecting, layer, efficient, grow, epitaxy, epitaxial, print

CATEGORIZED AS

- **Energy**
  - Other
- **Engineering**
  - Engineering
  - Other
- **Materials & Chemicals**
  - Other
- **Semiconductors**
  - Assembly and Packaging
  - Design and Fabrication
  - Materials
  - Other
  - Processing and Production
- **Sensors & Instrumentation**
  - Other
  - Scientific/Research

RELATED CASES

2015-453-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Diamond On Nanopatterned Substrates

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