RASP: FPGA/CPLD Technology Mapping And Synthesis Package

Tech ID: 29873 / UC Case 2018-336-0

SUMMARY

Researchers led by Jason Cong from the Computer Science Department at UCLA have developed a general synthesis and mapping system for SRAM-based FPGAs.

BACKGROUND

Field programmable gate arrays (FPGA) are configurable chips in which the user can implement their designs to execute particular tasks. The configurable blocks in an FPGA can have their function specified using a look up table (LUT). Due to their flexibility and configurability, FPGA's have adopted wide-spread use for rapid ASIC design and rapid system prototyping. To take advantage of these systems, users need a synthesis system that not only programs FPGAs but does so in an optimal way (ex. Delay and area minimization). However, there are many different commercially available FPGAs each of which has their own unique characteristics like number of LUTs, sizes, and connection patterns. This creates a need for a general synthesis system that can handle all the different FPGA designs rather than synthesis system for each FGPA. Currently, a general synthesis system does not exist.

INNOVATION

Researchers led by Jason Cong from the Computer Science Department at UCLA has developed a general synthesis and mapping system for SRAM-based FPGAs. They have created the RASP (Rapid System Prototyping) system that provides a flexible, general synthesis system that can optimally create LUT networks and then map them to different FPGA architectures. The flexibility lies not only in RASP's ability to map LUT's to different FPGA architectures, but it can also be loaded with different algorithms that optimize LUT network design according to objectives listed in the previous paragraph or a combination of them. Furthermore this system provides the flexibility to load different FPGA architectures in case if different ones are made in the future. RASP also provides the flexibility for experimentation at each sub-step of the synthesis and mapping process, which is useful in tuning the optimization for a particular objective. So far, RASP has been able to incoroporate FlowMap, FlowMap-R, FlowSYN, and CutMap mapping algorithms and then map them to LUT-based commercial FPGAs.

APPLICATIONS

- Optimizing synthesis of FPGAs
- Mapping LUT networks to different FPGA architectures

ADVANTAGES

- Flexibility
- Generalizability

CONTACT

UCLA Technology Development Group
ncd@tdg.ucla.edu
tel: 310.794.0558.

OTHER INFORMATION

KEYWORDS

FPGA, LUT, CPLD, programming, software, ASIC, configuration, gate arrays, chips, SRAM

CATEGORIZED AS

- **Computer**
  - Other
- **Semiconductors**
  - Other
- **Engineering**
  - Other

RELATED CASES

2018-336-0

UCLA Technology Development Group
10889 Wilshire Blvd., Suite 920,Los Angeles,CA 90095
https://tdg.ucla.edu
Tel: 310.794.0558 | Fax: 310.794.0638 | ncd@tdg.ucla.edu