A Plastic Synapse Based on Self-Heating-Enhanced Charge-Trapping in High-K Gate Dielectrics of Advanced-Node Transistors

Tech ID: 29822 / UC Case 2016-799-0

SUMMARY

UCLA researchers in the Department of Electrical Engineering and Computer Science have developed a novel way of implementing plastic synapses for neuromorphic systems applications by using charge-trapping advanced-node transistors.

BACKGROUND

Brain-inspired neuromorphic computing holds the promise to replace conventional von Neumann computers for cognitive applications. Neuromorphic computing systems feature distributed processors (e.g., electronic neurons or neuron devices), local memory (e.g., electronic synapses or synapse devices), and significantly more connections. This carries the potential for massively parallel processing power as compared with current architectures. To implement the neuromorphic system, the physical devices need to mimic the behavior of plastic synapses as in our brain. However, a compact and reliable physical device structure to implement the synapses is still lacking.

INNOVATION

Researchers at UCLA designed a novel way to implement synapses by utilizing advanced-node transistors which show charge-trapping behaviors in high-k gate dielectrics. Only three such transistors are needed to implement a single synapse. In addition, the conductance of the synapse can be tuned over more than two orders of magnitude. The synapse device, combined with complementary metal-oxide semiconductor (CMOS) neuron and control circuits, provides an adaptive learning and large-scale neuromorphic system.

APPLICATIONS

Physical implementation of neuromorphic computers

- Pattern recognition, including images and speech processing
- Smart robotics and self-driving cars that can understand and interact with the world in humanlike ways
- Medical sensors and devices that track individuals' signs over time, learning to adjust dosages or even catch problems early
- Smartphone applications that learn to anticipate what the user wants next

Neuromorphic chips for the study of neuroscience and brain

ADVANTAGES

Highly compact (3-transistor for one synapse)

Compatibility with large-scale integration (can be implemented by multiple existing transistor technologies)

- Highly uniform
- Highly reliable
- Highly scalable
- No extra material or process complexity

Capable of different learning behaviors by different signaling schemes

STATE OF DEVELOPMENT

CONTACT

UCLA Technology Development Group
ncd@tdg.ucla.edu
tel: 310.794.0558.

INTRODUCING
UC TechAlerts
New technology matches delivered to your email at your preferred schedule
SEARCH SAVE SEARCH
Learn More

INVENTORS

- Iyer, Subramanian

OTHER INFORMATION

KEYWORDS

Plastic synapse, synapse, charge trapping, high-k, gate dielectric, transistor, neuromorphic, self-heating

CATEGORIZED AS

- **Computer**
  - Hardware
  - Other
- **Semiconductors**
  - Design and Fabrication
  - Materials

RELATED CASES

2016-799-0

The UCLA researchers have proposed the signaling scheme to realize the synapse based on the charge-trapping transistors. Part of the device behaviors of the charge-trapping transistors have been published as a journal article.

RELATED MATERIALS

- F. Khan, E. Cartier, C. Kothandaraman, J. C. Scott, J. C. S. Woo, and S. S. Iyer, The Impact of Self-Heating on Charge Trapping in High-k-Metal-Gate nFETs, IEEE Electron Device Letters, 2015.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,585,643	03/10/2020	2016-799

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Flexible And Stretchable Interconnects For Flexible Systems And Flextrate(Tm)
- Power Distribution within Silicon Interconnect Fabric
- Intelligent Flexible Spinal Cord Stimulators For Pain And Trauma Management Through Neuromodulation
- Trademark: Flexible Fan Out Wafer Processing And Structure: Flextrate
- Network On Interconnect Fabric

UCLA Technology Development Group
10889 Wilshire Blvd., Suite 920,Los Angeles,CA 90095
https://tdg.ucla.edu
Tel: 310.794.0558 | Fax: 310.794.0638 | ncd@tdg.ucla.edu

© 2018 - 2020, The Regents of the University of California
Terms of use
Privacy Notice