Quarter-Rate Serial Link Receiver with Low Aperture Delay Samplers for High Data Rate Applications

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ABSTRACT

Researchers at the University of California, Davis have developed a quarter-rate serial link receiver with low aperture delay samplers for use in high-speed serial link interconnects in network systems. This receiver decreases the parasitic capacitances that result from threshold adjustments and can drastically decrease the amount of power required for high data rate applications.

FULL DESCRIPTION

Serial links are used for connections between chips in networked systems and are important in multimedia sharing, cloud computing, virtual reality (VR) and other high use network systems. Traditional serial link receivers use equalizers, for example, half rate continuous-time linear equalizer (CTLE) with decision feedback equalizer (DFE), to reduce inter-symbol interference (ISI). Next-generation data rates, however, will require higher speeds and the currently employed half rate receivers will be inefficient and require more power.

Researchers at the University of California, Davis have designed a quarter-rate serial link receiver with much lower aperture delays in the samplers for use in high date rate applications. This design ensures that almost no noise affects the data and that the power consumption of the serial link is unchanged due to the increased speeds by utilizing offset calibration and DFE threshold adjustment. The full quarter-rate architecture saves more than a half of power consumption compared to half-rate architecture and the combination of DFE threshold adjustment and the sampler offset calibration improves system performance without introducing excessive parasitic capacitance. This new scheme has been successfully simulated and confirmed to achieve better eye-open performance while consuming less power compared to traditional half rate equalization.

APPLICATIONS

- Technologies that require a quasi-noiseless transmission of data within a networked system
- Decreasing the latency and power usage in virtual reality headsets and other wireless devices
- Improving energy efficiency and performance of cloud computing clusters

FEATURES/BENEFITS

- Decreases the power consumption of a serial link by taking away unnecessary parasitic capacitances
- Improved noise reduction due to threshold adjustment and offset calibration

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	11,018,845	05/25/2021	2018-495
United States Of America	Published Application	20210160043	05/25/2021	2018-495

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OTHER INFORMATION

KEYWORDS

serial link receiver, networked systems, half rate continuous-time linear equalizer, CTLE, decision feedback equalizer, DFE, inter-symbol interference, ISI, parasitic capacitance, high data rate application, high-speed serial link

CATEGORIZED AS

- **Communications**
  - Networking

RELATED CASES

2018-495-0

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