Power Distribution within Silicon Interconnect Fabric

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SUMMARY

UCLA researchers in the Department of Electrical Engineering have developed a novel method of powering systems on silicon interconnect fabrics for integration of packageless processors.

BACKGROUND

Over the past two decades, silicon chips have decreased in size by 1000x, while packages on circuit boards have only shrunk by 4x. This will eventually limit scaling of integrated circuits and subsequent processor performance. A solution is the invention of platforms for packageless integration of heterogeneous dies, such as silicon interconnect fabric (Si-IF), exhibiting significant improvements in thermal and electrical properties. However, novel power distribution networks for Si-IF must be designed for successful further innovation in this field.

INNOVATION

Professor Iyer and coworkers have developed a novel method of powering silicon interconnect fabric (Si-IF), a novel platform for heterogeneous systems integration. In this approach, a series of copper stubs are used to connect the back of the Si-IF to the socket. The front of the Si-IF is then powered using through wafer vias (TWVs), which penetrate the silicon substrate. This proposed network demonstrated a voltage drop of 298 µV (distributed voltage of 12V), can distribute multiple voltage domains, and only dissipated 248 mW of power.

APPLICATIONS

Power distribution network for high power systems integrated on silicon interconnect fabric

ADVANTAGES

- Low power dissipation
- Low voltage drop
- Multiple voltage domains possible

STATE OF DEVELOPMENT

A silicon interconnect fabric sample with 63,600 mm^2 effective area can be powered using this power distribution network. Through wafer vias and copper stub parameters were optimized, resulting in a power distribution network with a voltage drop of 298 µV (distributed voltage of 12V) that supports distribution of multiple voltage domains of 12V and 3.3V, and only dissipated 248 mV of power.

RELATED MATERIALS

- Saptadeep Pal, D. Petrisko, A. Bajwa, P. Gupta, S. S. Iyer, and R. Kumar "A Case for Packageless Processors", 24th IEEE International Symposium on High-Performance Computer Architecture (HPCA), February 24-28, 2018, Vienna, Austria.
- B. Vaisband, A. Bajwa, and S. S. Iyer, “Network on Interconnect Fabric,” Proceedings of the IEEE International Symposium on Quality Electronic Design, March 2018.
- SivaChandra Jangam, S. Pal, A. Bajwa, S. Parmarti, P. Gupta and S. S. Iyer, "Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme", Proc. of 67th IEEE Electronic Components and Packaging Technology (ECTC) 2017, Orlando, FL, pp. 86-94. doi: 10.1109/ECTC.2017.246

PATENT STATUS

Country	Type	Number	Dated	Case

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INVENTORS

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OTHER INFORMATION

KEYWORDS

silicon interconnect fabric, power distribution network, packageless processors,

CATEGORIZED AS

- **Engineering**
  - Engineering
- **Nanotechnology**
  - Electronics
- **Semiconductors**
  - Design and Fabrication

RELATED CASES

2018-337-0

United States Of America	Issued Patent	11,257,746	02/22/2022	2018-337

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Flexible And Stretchable Interconnects For Flexible Systems And Flextrate(Tm)
- A Plastic Synapse Based on Self-Heating-Enhanced Charge-Trapping in High-K Gate Dielectrics of Advanced-Node Transistors
- Intelligent Flexible Spinal Cord Stimulators For Pain And Trauma Management Through Neuromodulation
- Trademark: Flexible Fan Out Wafer Processing And Structure: Flextrate
- Network On Interconnect Fabric

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