# A Digital Polar and a ZVS Contour Based Hybrid Power Amplifier

Tech ID: 28976 / UC Case 2012-107-0

## SUMMARY

Researchers in the UCLA Department of Electrical Engineering have created a hybrid digital polar and zero switching voltage (ZVS) contour power amplifier, offering higher efficiency for up to 36 dB peak-to-average ratio.

## BACKGROUND

Traditional power amplifiers are biased in order to maximize their efficiency at a given operating power. However, this makes them less efficient at lower power levels.Both high and low power levels can be important in wireless communications, where a large peak to average power ratio is common.Other hybrid approaches are theoretically efficient in their given power regimes, but high bandwidth modulations can suffer from supply regulator inefficiency.

## INNOVATION

Researchers in UCLA's Department of Electrical Engineering have built upon recent power amplifier innovations to create a hybrid digital polar and zero switching voltage (ZVS) contour power amplifier. This hybrid system has the potential to double the efficiency of traditional RF transmitters, making it ideal for use in wideband digital communications.The contour amplifier allows for high efficiency below the 10 dB back-off, while the digital polar amplifier can easily attain up to 36 dB peak-to-average ratio (PAR).

## APPLICATIONS

Power amplifiers in wireless communications like WLAN, LTE, and WIMAX

## ADVANTAGES

- ZVS contour amplifier offers high efficiency in the low (<10 dB) back-off PAR regime
- Digital polar amplifier offers high efficiency in the 10-36 dB PAR regime
- High average efficiency, benefiting large personal mobile radio (PMR) signals like those used in orthogonal frequency digital multiplexing (OFDM)

## STATE OF DEVELOPMENT

Researchers at UCLA's department of Electrical Engineering are currently developing a proof-of-concept CMOS chip based on 130 nm CMOS architecture in order to validate their detailed simulations and theoretical foundations for this technology.

## RELATED MATERIALS

- N. Singhal, N. Nidhi, R. Patel, S. Pamarti, "A 19 dBm 0.13µm CMOS parallel class-E switching PA with minimal efficiency degradation under 6 dB back-off," IEEE Transactions on Microwave Theory and Techniques," vol. 59, no. 6, July 2011, pp. 1589-98.1
- N. Singhal, N. Nidhi, S. Pamarti, "A Power Amplifier with Minimal Efficiency Degradation under back-off," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, pp. 1851-54, 2010.2

## PATENT STATUS

| Country | Type | Number | Dated | Case |
|---|---|---|---|---|
| United States Of America | Issued Patent | 9071204 | 06/30/2015 | 2012-107 |

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## INVENTORS

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## OTHER INFORMATION

### KEYWORDS

Peak-to-average power ratio, power amplifier (PA), zero voltage switching (ZVS), hybrid power amplifier, wireless communications

### CATEGORIZED AS

- **Communications**
  - Other
- **Materials & Chemicals**
  - Electronics Packaging

### RELATED CASES

2012-107-0

## ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Method to Obtain Sharp Programmable Filters Using Simple Passive Switched-Resistor Circuits



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