Resistive Memory Write and Read Assistance Using Negative Differential Resistance Devices

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SUMMARY

UCLA researchers in the Department of Electrical Engineering have developed a new design of read and write circuitry using negative differential resistance devices to improve the performance of resistive memories.

BACKGROUND

Emerging non-volatile resistive memories including phase-change memory (PCM), spin-transfer torque magnetic random access memory (STT-MRAM), resistive switching RAM (RRAM), etc. are promising for storage, cache, and computing in future. Among these, STT-MRAM is especially promising due to its high endurance, and relative fast access time. However, STT-MRAMs suffer from three main challenges: 1) high write energy, 2) low sensing margin (read difficulty), and 3) susceptibility to read disturbance.

INNOVATION

UCLA researchers proposed a new memory read and write circuitry that can solve all the three problems above. This new design uses negative differential resistance (NDR) devices in series with the memory cell write or read current path. The use of pre-charge transistor and pre-charge pulse sequence is employed to maximize the usefulness of the NDR device. A NDR can also be shared and connected to the several bit-lines that share a sense amplifier.

APPLICATIONS

Improve the performance of resistive memories:

- Phase-change memory (PCM)
- Magnetic RAM (MRAM) including STT-MTJs, magnetoelectric RAM (MeRAM)
- Resistive switching RAM (RRAM) including conductive bridging memory (CBM)

ADVANTAGES

- Decrease write energy, by write current cut-off upon cell switching
- Improve sensing margin, thus reduce read difficulty, delay, energy, and errors
- Reduce read disturbance
- Reduce sensing circuit size (used transistor size), and simplifying sensing circuit design (possible to eliminate need for sense amplifiers)
- Minimal circuit overhead, one NDR device can be shared and connected to several bit-lines
- Can be applied to other resistance-changing memory technologies such as RRAM, PCM, MeRAM

STATE OF DEVELOPMENT

The UCLA researchers have proposed and simulated a new memory write and read circuitry using negative differential resistance (NDR) devices. Circuit simulations on STT-MRAM have shown write energy reduction of 2x, read margin improvements of over 3x, and read disturbance reduction over 100,000x. Also, the device specification for NDR devices is also low (peak-to-valley ratio > 3) for significant improvement in write energy efficiency (> about 1.8×) and read margin (> about 2×).

PATENT STATUS

Country	Type	Number	Dated	Case

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OTHER INFORMATION

KEYWORDS

Non-volatile memory, resistive memory, phase-change memory, PCM, magnetic random access memory, MRAM, spin-transfer torque random access memory, STT-MRAM, magnetoelectric random access memory, MeRAM, resistive switching random access memory, RRAM, conductive bridging memory, CBM, write energy, sensing margin, read margin, read disturbance, negative differential resistance, NDR

CATEGORIZED AS

- **Computer**
  - Hardware
- **Nanotechnology**
  - Electronics
- **Semiconductors**
  - Design and Fabrication

RELATED CASES

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