A CMOS Compatible Fully-Integrated Switched-Domain Power Inverter Circuit

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BACKGROUND

Modern mobile applications strive for the complete integration of all communication systems in CMOS. Unfortunately, it is conventionally difficult to efficiently generate high levels of RF power in scaled CMOS largely due to the inherently low voltage ratings of core transistors. To realize high output power with ~1V transistors, power combining techniques have been proposed whereby the output of several low-voltage power amplifier (PA) cells are combined via inductive transformers. However, power combining relies on ultra-thick metal that still carries large ohmic and substrate losses. These AC-AC losses, combined with the DC-AC losses of the PAs themselves, and the DC-DC losses of the battery-connected power converters, result in limited total transmitter efficiencies. Even modern digital PA techniques such as RF-DACs, digital Doherty, and digital out-phasing, which have been proposed to leverage the excellent switch performance of scaled transistors and offer reconfigurable operation, still require battery-connected DC-DC converters and RF transformers/power combiners, both of which result in cascaded losses.

TECHNOLOGY DESCRIPTION

Researchers at UC San Diego have invented a DC-RF power inverter that efficiently synthesizes high-voltage RF waveforms directly from a battery voltage using thin-oxide CMOS switches. Instead of stacking transistors or employing large inductive transformation ratios, high output power is generated by switching individual class-D power amplifier (PA) cells in a 2-phase house-of-cards (HoC) topology to provide voltage addition of the cells outputs without exceeding device voltage ratings, effectively resulting in a solid-state RF impedance transformer. High-efficiency at back-off is then achieved by capacitively combining the output of two HoC networks nominally set to generate different amplitudes, enabling voltage-mode Doherty-like back-off without a bulky transmission line. The PA is implemented in 65nm bulk LP CMOS, operates from 4.8V, and provides a battery-to-RF efficiency above 40% at both 23dBm and 6dB back-off at 720MHz.

APPLICATIONS

The technology is suitable for broad range of applications, including: RFpower amplifiers (PA), 20kHz audio amplifiers, and 50-60 Hz power inverters. The above technology will have immediate application in portable electronics by leveraging an all CMOS design (no separate PA’s or transformers) to reduce the cost and complexity of hardware while also extending battery life.

ADVANTAGES

The key advantage of the proposed technology is CMOS compatibility, high efficiency, which equates to longer battery life and operational-time.

STATE OF DEVELOPMENT

Research stage with a working prototype

INTELLECTUAL PROPERTY INFO

This technology is patent pending and available for commercial development.

CONTACT

University of California, San Diego
Office of Innovation and Commercialization
innovation@ucsd.edu
tel: 858.534.5815.



OTHER INFORMATION

KEYWORDS

DC-RF power inverter, CMOS switches,RF power amplifiers, portable electronics

CATEGORIZED AS

- **Energy**
  - Transmission
- **Engineering**
  - Engineering

RELATED CASES

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PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Published Application	20180097486	04/05/2018	2016-088

University of California, San Diego
Office of Innovation and Commercialization
9500 Gilman Drive, MC 0910, ,
La Jolla,CA 92093-0910

Tel: 858.534.5815
innovation@ucsd.edu
https://innovation.ucsd.edu
Fax: 858.534.7345

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