A Novel Computer Architecture Based Upon Memory Enhanced Logic Gates

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TECHNOLOGY DESCRIPTION

Given here is a non-Turing Machine architecture for computer hardware capable of solving non-polynomial time problems in polynomial time. Typically, with each added bit of input complexity, a computational system must grow in complexity in an exponential fashion. For instance, two input bits give four possible bit states (00, 01, 10, 11) but 3 input bits give eight possible states, and 4 input bits give 16 states. This quickly scales with 8 bits giving 1,024 possible bit combinations and in the case of RSA encryption, 2,048 bits gives… (I'm not exactly sure, but it's a lot!)

Rather than approach computing in the traditional brute-force approach, memory elements are integrated into the logic, yielding much simpler circuits which operate in both a forward and reverse mode until a satisfactory solution is reached, yielding an equilibrium state for a given design. In this way, traditionally non-polynomial time problems can be solved with polynomial circuit implementations and much faster computing is possible.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,911,080	03/06/2018	2016-008
United States Of America	Published Application	20170316309	11/02/2017	2016-008
Patent Cooperation Treaty	Published Application	2017011463	01/19/2017	2016-008

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OTHER INFORMATION

KEYWORDS

software, computer architecture, logic gates, memory

CATEGORIZED AS

- Computer
  - Software

RELATED CASES

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