A Self-Organized Critical CMOS Circuit for Computation and Information Processing

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SUMMARY

UCLA researchers in the Department of Electrical Engineering have developed a novel system architecture for solving optimization problems faster using chaos or self-organized criticality to generate a matrix of bits for computation.

BACKGROUND

Conventional computers are efficient in solving sequential arithmetic problems but they are inefficient in solving problems with many interacting variables. Such problems usually do not have exact analytical solutions and are often deemed non-deterministic polynomial-time hard (NP-hard) for conventional computers. Annealing approaches have been proposed but generally suffer from slow processes and lack the means for reliably reading out solutions. Meanwhile, demand is increasing for computational systems that can solve such complicated problems, as they arise in the form of image recognition, modeling physical systems and optimizing large systems.

INNOVATION

The proposed system architecture leverages recent breakthroughs in the understanding of the self-organized criticality phase in complex dynamics systems to solve optimization problems much faster. The system converges to a global minimum much faster than conventional simulated and chaotic annealing approaches implemented in software.

APPLICATIONS

Faster optimization problem solver in any computer.

ADVANTAGES

- Outperforms conventional simulated or chaotic annealing implemented in software
- Ability to provide intermediate candidate solutions, which chaotic annealers cannot do

STATE OF DEVELOPMENT

The system has been validated in circuit simulations. Testing of a successfully fabricated device is underway.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,147,045	12/04/2018	2013-714

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Vertical-Stacked-Array-Transistor (VSAT) for Nonvolatile Memory Devices
- Magnetic Memory Bits with Perpendicular Magnetization Switched By Current-Induced Spin-Orbit Torques
- Vsat Structure for Nonvolatile Memory Device
- A Read-Disturbance-Free Nonvolatile Content Adressable Memory

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OTHER INFORMATION

KEYWORDS

self-organized criticality, computation, nanosystem, system architecture, complex dynamical system, optimization problems, CMOS, complementary metal-oxide-semi conductor, integrated circuit

CATEGORIZED AS

- **Computer**
  - Hardware
- **Engineering**
  - Engineering
- **Nanotechnology**
  - Electronics

RELATED CASES

2013-714-0

▶ Anti-Ferromagnetic Magneto-Electric Spin-Orbit Read Logic

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