Novel Processing Method for Group III-V Semiconductor Surfaces

Tech ID: 24867 / UC Case 2014-816-0

BRIEF DESCRIPTION

A processing method for group III-V semiconductor surfaces prior to high-dielectric constant dielectric deposition by atomic layer deposition (ALD) or another deposition method.

BACKGROUND

Complementary metal-oxide-semiconductor (CMOS) is a technology for developing integrated semiconductors and transistors that amplify or switch electrical signals. CMOS transistors have been using silicon channels that limit capacitance density and induce high-voltage leaks. Group III-V compounds are semiconducting materials that feature higher carrier mobilities, increased capacitance density, and less voltage leakage than silicon channels.

DESCRIPTION

Researchers at UC Santa Barbara have developed a processing method for group III-V semiconductor surfaces prior to high-dielectric constant dielectric deposition by atomic layer deposition (ALD) or another deposition method. The method exposes the III-V surface to alternating or repeated cycles of a remote or direct plasma, which may be a plasma of nitrogen or hydrogen or another gas, or a mixture of such gases, and a titanium precursor. This provides the low defect densities and extremely high capacitance densities without reaching limitations posed by high leakage currents.

ADVANTAGES

- Extremely high capacitance density
- Reduces high leakage currents
- Low defect densities

APPLICATIONS

- Semiconductors
- Transistors

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,190,266	11/17/2015	2014-816

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OTHER INFORMATION

KEYWORDS

group III-V, semiconductors, transistors

CATEGORIZED AS

- **Semiconductors**
  - Processing and Production

RELATED CASES

2014-816-0

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