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GaN-based Vertical Metal Oxide Semiconductor and Junction Field Effect Transistors

Tech ID: 24820 / UC Case 2014-718-0

BRIEF DESCRIPTION

The first true vertical GaN-based transistors, where gating is also performed on electrons traveling perpendicular to the surface in a vertical channel.

BACKGROUND

In recent years, GaN-based transistors have attracted much attention because of their high-power performance. The effectiveness of lateral GaN on silicon-based high electron mobility transistors (HEMTs) has been demonstrated through their commercial availability. However, these devices are fairly complex and expensive to fabricate, and have a large device area. One method to alleviate some of these issues is to replace lateral GaN transistors with vertical GaN-based transistors.

DESCRIPTION

Researchers have designed the first true vertical GaN-based transistors, where gating is also performed on electrons traveling perpendicular to the surface in a vertical channel. Drift region spreading resistance is extremely low, and is achieved by inserting a two-dimensional electron gas produced at a heterojunction within the device on either side of the channel. This method significantly improves the device performance because it utilizes the full area of the drift region for conduction. The gating of the device is variable, allowing for the creation of a metal oxide semiconductor field effect transistor (MOSFET) or a junction gate field effect transistor (JFET). In addition, to reduce resistance and chip cost, the electrically active area of the device can be equal to the geometric chip area.

ADVANTAGES

- Reduced chip cost due to small chip size
- Improved device performance over any current GaN-based transistors on the market
- · High switching speed and extremely low contact resistance and drift resistance

APPLICATIONS

- Metal oxide semiconductor field effect transistors (MOSFETs)
- · Junction gate field effect transistors (JFETs)

CONTACT

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INVENTORS

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OTHER INFORMATION

KEYWORDS

indSSL, GaN, transistor,

MOSFET, JFET, indfeat,

indmicroelec

CATEGORIZED AS

- Energy
 - ► Transmission
- ► Materials & Chemicals
 - ► Electronics Packaging
- Semiconductors
 - Design and

Fabrication

Materials

RELATED CASES

2014-718-0

PATENT STATUS

| Country | Type | Number | Dated | Case |
|--------------------------|---------------|------------|------------|----------|
| United States Of America | Issued Patent | 10,312,361 | 06/04/2019 | 2014-718 |

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- ► High-Quality N-Face GaN, InN, AIN by MOCVD
- ▶ Defect Reduction in GaN films using in-situ SiNx Nanomask
- ▶ A Structure For Increasing Mobility In A High-Electron-Mobility Transistor
- ▶ Improved Fabrication of Nonpolar InGaN Thin Films, Heterostructures, and Devices
- ▶ Methods for Locally Changing the Electric Field Distribution in Electron Devices
- ▶ Technique for the Nitride Growth of Semipolar Thin Films, Heterostructures, and Semiconductor Devices
- ► (In,Ga,Al)N Optoelectronic Devices with Thicker Active Layers for Improved Performance
- Novel Current-Blocking Layer in High-Power Current Aperture Vertical Electron Transistors (CAVETs)
- ▶ Iii-N Transistor With Stepped Cap Layers
- ▶ III-N Based Material Structures and Circuit Modules Based on Strain Management

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