GaN-based Vertical Metal Oxide Semiconductor and Junction Field Effect Transistors
Tech ID: 24820 / UC Case 2014-718-0

BRIEF DESCRIPTION
The first true vertical GaN-based transistors, where gating is also performed on electrons traveling perpendicular to the surface in a vertical channel.

BACKGROUND
In recent years, GaN-based transistors have attracted much attention because of their high-power performance. The effectiveness of lateral GaN on silicon-based high electron mobility transistors (HEMTs) has been demonstrated through their commercial availability. However, these devices are fairly complex and expensive to fabricate, and have a large device area. One method to alleviate some of these issues is to replace lateral GaN transistors with vertical GaN-based transistors.

DESCRIPTION
Researchers have designed the first true vertical GaN-based transistors, where gating is also performed on electrons traveling perpendicular to the surface in a vertical channel. Drift region spreading resistance is extremely low, and is achieved by inserting a two-dimensional electron gas produced at a heterojunction within the device on either side of the channel. This method significantly improves the device performance because it utilizes the full area of the drift region for conduction. The gating of the device is variable, allowing for the creation of a metal oxide semiconductor field effect transistor (MOSFET) or a junction gate field effect transistor (JFET). In addition, to reduce resistance and chip cost, the electrically active area of the device can be equal to the geometric chip area.

ADVANTAGES
• Reduced chip cost due to small chip size
• Improved device performance over any current GaN-based transistors on the market
• High switching speed and extremely low contact resistance and drift resistance

APPLICATIONS
• Metal oxide semiconductor field effect transistors (MOSFETs)
• Junction gate field effect transistors (JFETs)

PATENT STATUS
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<td>United States Of America</td>
<td>Issued Patent</td>
<td>10,312,361</td>
<td>06/04/2019</td>
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ADDITIONAL TECHNOLOGIES BY THESE INVENTORS
• Achieving “Active P-Type Layer/Layers” In III-Nitride Epitaxial Or Device Structures Having Buried P-Type Layers
• High-Quality N-Face GaN, InN, AlN by MOCVD
• Defect Reduction in GaN films using in-situ SiNx Nanomask
• Laser Diode With Tunnel Junction Contact Surface Grating
▶ High Mobility Group-III Nitride Transistors with Strained Channels
▶ A Structure For Increasing Mobility In A High-Electron-Mobility Transistor
▶ Fabrication of Relaxed Semiconductor Films without Crystal Defects
▶ Improved Fabrication of Nonpolar InGaN Thin Films, Heterostructures, and Devices
▶ Methods for Locally Changing the Electric Field Distribution in Electron Devices
▶ Near-Infrared, Flip-Chip, TCO-Clad, InGaN Quantum Dot Laser Diode
▶ Incorporating Temperature-Sensitive Layers in III-N Devices
▶ Technique for the Nitride Growth of Semipolar Thin Films, Heterostructures, and Semiconductor Devices
▶ Enabling Epitaxial Growth On Thin Substrates
▶ (In,Ga,Al)N Optoelectronic Devices with Thicker Active Layers for Improved Performance
▶ Novel Current-Blocking Layer in High-Power Current Aperture Vertical Electron Transistors (CAVETs)
▶ III-N Transistor With Stepped Cap Layers
▶ Polarization-Doped Field Effect Transistors with Increased Performance
▶ Wafer Bonding for Embedding Active Regions with Relaxed Nanofeatures
▶ III-N Based Material Structures and Circuit Modules Based on Strain Management