Capacitive Passive Mixer Baseband Receiver With Broadband Harmonic Rejection

Tech ID: 24769 / UC Case 2015-075-0

BACKGROUND

Broadband receivers for applications such as TV band tuners, multi-band cellular, or cognitive radio and software defined radio often employ a passive mixer harmonic rejection down-converter for high linearity and harmonic folding rejection [1-6]. Conventionally, a multi-phase passive mixer with either transconductance [1] or resistive weighting [2-5] is employed to approximate a synthetic sinusoidal down-converting clock. Such conventional harmonic rejection mixer (HRM) designs suffer from device and resistive noise limiting receiver sensitivity, as well as nonlinear distortion due to voltage-dependent transconductance or switch resistance, and finite input impedance of transimpedance amplifiers. Noise-cancelling schemes compensate partially for the heightened noise levels due to resistive passive mixing [7] and incur greater circuit complexity. Furthermore, the vast majority of HRM designs [1-7] operate at relatively high power consumption levels limiting their use for mobile applications operating under stringent battery size and weight constraints.

The present invention fundamentally advances over the prior art in the use of charge-based (or capacitive) passive HRM, rather than transconductance-based and other active HRM (e.g., US Patent 7,738,851 [8]) or resistance-based passive HRM (e.g., US Patent 7,738,851 [9]). Distinct advantages of the charge-based HRM invention, overcoming the above shortcomings, are described below.

TECHNOLOGY DESCRIPTION

The present invention implements capacitive HRM in which a capacitor array, switched by multi-phase local oscillator (LO) clock signals, implements harmonic mixing of the signal with sinusoidal weights. Since the weights are implemented by capacitance sizing, thermal noise is reduced, and linearity is improved over conventional implementations employing transconductance or resistive weighting. Furthermore, as the down-conversion is charge based, the device size of the down-conversion passive mixer can be reduced, and the input impedance requirements of the TIA can be relaxed, significantly reducing baseband receiver power consumption.

Different embodiments of the capacitor array and LO clocking can be used for different applications in capacitive passive mixer and baseband receiver harmonic rejection. These include an N-path filtering sinusoidal capacitor array with single-phase clocking, and a thermometer-encoded sinusoidal capacitor array with incremental phase coding. These and other embodiments in accordance with the present invention minimize noise, minimize capacitor array layout area, and minimize power consumption by allowing for small passive mixer switch size.

APPLICATIONS

A description of several examples of embodiments follows. N-Path Filtering Capacitive HRM: Fig. 1 shows one embodiment of the invention, illustrating an *N*-path filtering harmonic rejection mixer (HRM), where *N* is the number of phases in the local oscillator (LO), and correspondingly the number of capacitors switched by the LO, implementing sinusoidal modulation of the RF input in *N* discrete periodic steps.

The *N*-phase sinusoidally weighted mixing eliminates harmonic folding of the signal spectrum into baseband, at all harmonics of the LO frequency up to order *N*-2. For the example *N* = 16 shown, all LO harmonics of orders ranging from 2^{nd} to 14^{th} are suppressed. Owing to superior matching in capacitance device sizing across a typical integrated circuit, the capacitive HRM allows for greater (> 65 dB) suppression of these LO harmonics than comparably sized transconductance or conductance weights using CMOS or other active elements.

The architecture supports both real (single-phase signal path) and complex (in-phase *I* and quadrature *Q* signal paths) mixing, with only one path (*I* path) shown. The *I/Q* paths are mirror-symmetric with cosine and sine weighted capacitive arrays, respectively. Furthermore, all bias

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OTHER INFORMATION

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RELATED CASES
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and control signals including clock can be shared for *I/Q* paths, which results in low power consumption.

As a proof of concept, an example embodiment with N = 16 phases is shown in Fig. 1, with a 16-phase clock, and with 16 cosine (or sine) weighted capacitors. In general the N-phase clock for the LO may be generated by digital logic, or through use of a phased-locked loop (PLL), delay-locked loop (DLL), etc. Sinusoidal weighting for harmonic modulation is implemented as the ratio of the switched capacitances and the transimpedance amplifier (TIA) feedback capacitance. For optimal matching in capacitive weighting, all weights are implemented in multiples of equally sized capacitance units. Targeting better than -60dB harmonic rejection, the discrete realizations of capacitance values for the sinusoidal weighting in integer and half fractional units are illustrated in Fig. 1, where half units are implemented by series combination of two capacitor units. The 16-phase modulation sine wave is encoded double differentially, each phase with 4 capacitors, such that the RF input as well as the baseband TIA see a constant capacitance load throughout all phases of the capacitive switching. Charge injected by the harmonic reject mixing capacitive array is summed and bandpass filtered by the TIA.

Fig. 2 illustrates an example embodiment of CMOS circuit implementation of a 16-phase, 16-path (N = 16) capacitive HRM *I/Q* direct-down-converter, with transimpedance amplifier. Switches are implemented using single nMOS transistors, although pMOS transistors or combination of nMOS and pMOS transistors may also be used. The switches are shown connected to the TIA side (baseband receiver); however in alternative embodiments the switches may instead be placed on the other side of the capacitors, connecting directly to the RF input.

Unlike conventional conductance-based passive HRM [2-6], sizing of the switches is not critical for matching, dynamic range, and linearity, and can be minimized for low power dissipation. Specifically, the R_{on} switch resistance has minimal effect on the down-converted signals below the TIA low-pass cut-off frequency. In addition to power savings, minimum switch sizing reduces the impact of charge injection and clock feed-through. Furthermore, switch mismatch does not limit harmonic rejection to first order. Hence, minimum transistor length sizing may be chosen for the switches. Switch transistor width can be chosen in consideration of the turn on time of the switch and the amount of charge transferred to the TIA, but is significantly narrower than conductance-based passive HRM. The compact sizing of the switch transistors leads to great savings in area and power consumption. An additional nMOS resistance, R_H, in common for all phases in the array is inserted for uniform low-pass filtering of switching noise. If desired, this single common resistor may be implemented with a large size nMOS for reliable control over cut-off frequency, along with the TIA bias current.

Thermometer-encoded Capacitive Array for Capacitive HRM: Fig. 3 illustrates an alternative embodiment of the invention which reduces the number of capacitors and simplifies the construction of the LO clock phases, leading to lower power and reduced area. This embodiment applies thermometer-encoding of the N-phase sine wave from discrete amplitudes into smaller discrete incremental and decremental steps, where corresponding portions of a single array of capacitors are activated and deactivated in turn for each phase of the LO. The smaller number of discrete steps reduces the range of capacitor units hence reducing the total capacitance area. The thermometer-encoded single-capacitor-block array for all 16-phases of an *I* or *Q* path is shown in Fig. 3. A sinusoidal time-varying signal-coupling capacitance is thus instantiated, in which the incremental differential capacitance is added (connected to the positive signal polarity) or subtracted (connected to the negative signal polarity) between consecutive phases. The corresponding LO clock thermometer-encoded driving waveforms are shown in Fig. 4 for a 16-phase HRM. The thermometer-encoded single-capacitor-block array also lowers power consumption owing to parallel switching: switches at each capacitor in Fig. 3 are activated in parallel, reducing the size requirements of the switch such that the LO driving power consumption can be minimized.

These and various other alternative embodiments of the capacitive HRM and baseband receiver may be devised, each offering low-power, high-linearity and low-noise alternatives to conventional transconductance or conductance weighting in HRM. For instance, the TIAs in Figs. 1, 2 or 3 may be replaced by alternative embodiments for charge-based summing, the simplest of which is an open circuit followed by a high-input impedance voltage buffer such as a source follower. Multi-stage extensions to capacitive HRM, in which modules performing harmonic modulation are cascaded to implement higher number of phases with fewer components, are also within the scope of the invention. An example is suggested in the passive HRM of [9], in which conductance-based mixing may be replaced with capacitive mixing.

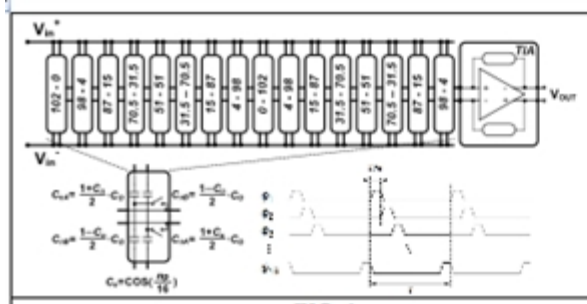


FIG. 1

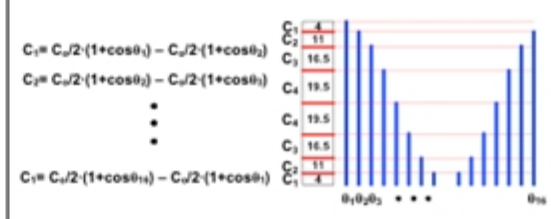


FIG. 5

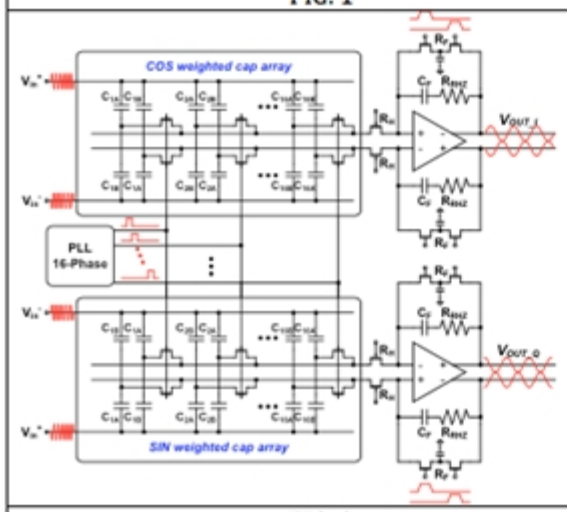


FIG. 2

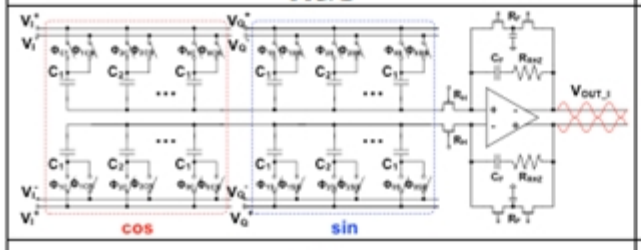


FIG. 3

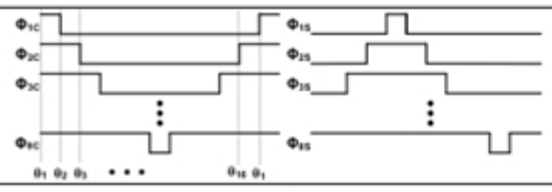


FIG. 4

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PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,876,518	01/23/2018	2015-075

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