

ENHANCED PATTERNING OF INTEGRATED CIRCUITS

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PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,347,501	07/09/2019	2015-085

BRIEF DESCRIPTION

Information and communication technologies rely on integrated circuits (ICs) or "chips." Increased integration has improved system performance and energy efficiency, and lowered the manufacturing cost per component. Moore's Law predicts that the number of transistors on an IC will double every two years, yet industry experts predict that we are reaching economic limits of traditional circuit patterning processes.

Photolithographic patterning is best suited to print linear features that are evenly spaced. The smaller or more complex the shape, the more likely the printed pattern will be blurred and unusable. Although multiple-patterning techniques can be used to increase feature density on ICs, they bring a high additional cost to the process. This means that the most advanced ICs available today have a high density of features, but are restricted to having simple patterns and are increasingly expensive to produce. Without innovations in production techniques, Moore's Law will reach its end in the near future.

To address this issue, researchers at UC Berkeley have developed a one-step method to increase feature density on chips. This method is capable of achieving arbitrarily small feature size, and self-aligns to pre-existing features on the surface formed by other techniques.

SUGGESTED USES

- » Producing ICs with complex patterns
- » Producing ICs with increased feature density

ADVANTAGES

- » One additional step rather than many
- » Self-aligns to pre-existing surface features
- » Produces features smaller than the current resolution limit
- » Doubles the density of features
- » Final feature sizes can be fine-tuned

RELATED MATERIALS

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OTHER INFORMATION

CATEGORIZED AS

- » **Communications**
- » Optical
- » Other
- » **Computer**
- » Hardware
- » **Semiconductors**
- » Processing and Production

RELATED CASES

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