A Reconfigurable Mostly-Digital Delta-Sigma ADC with a Worst-Case FOM of 160 dB

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TECHNOLOGY DESCRIPTION

Disclosed here is a second-generation mostly-digital background-calibrated oversampling ADC based on voltage controlled ring oscillators {VCROs). Its performance is in line with the best .4.E modulator ADCs published to date, but it occupies much less circuit area, is reconfigurable, and consists mainly of digital circuitry. Enhancements relative to the first-generation version include digitally background-calibrated open-loop V/ I convention in the VCRO to increase ADC bandwidth and enable operation from a single low-voltage power supply, quadrature coupled ring oscillators to reduce quantization noise, digital over-range correction to improve dynamic range and enable graceful overload behavior, and various circuit-level improvements. The ADC occupies 0.075 mm2 in a 65 nm CMOS process and operates from a single 0.9--1.2 V supply. Its sample-rate is tunable from 1.3 to 2.4 GHz over which the SNDR spans 71-75 dB, the bandwidth spans 5-37.5 MHz, and the minimum SNDR+ IOlog(bandwidth/power dissipation) figure of merit (FOM) is 160 dB.

INTELLECTUAL PROPERTY INFO

This technology is currently patent pending with rights available.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,397,691	07/19/2016	2013-317

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OTHER INFORMATION

CATEGORIZED AS

- Communications
  - Wireless

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