Self-Limiting CVD of Silicon Monolayer for Preparation of Subsequent Silicon or Gate Oxide ALD on III-V Semiconductor and Metal Surfaces

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BACKGROUND

Two of the leading materials considered for use in post silicon n-channel regions of planar-FETs and finFETs are SiGe and InGaAs, as both of these alternatives contain high intrinsic electron mobilities. A broader range of channel materials allowing better carrier confinement and mobility could be employed if a universal control monolayer (UCM) could be atomic layer deposited (ALD) or self-limiting chemical vapor deposited (CVD) on multiple materials and crystallographic faces. The existing silicon ALD process is not self-limiting.

TECHNOLOGY DESCRIPTION

In a related invention (2014-117), this team of inventors provided an improved procedure for the self-limiting and saturating atomic layer deposition (ALD) and self-limiting and saturating chemical vapor deposition (CVD) of a silicon seed layer on popular wafer substrates of varying alloy compositions (i.e. indium gallium arsenide, indium gallium antiminide, indium gallium nitride, and silicon-germanium). Here, the researchers have extended their invention by dosing surface sites with chlorosilane precursors (SiCl4, Si2Cl6 and Si3Cl8) at high pressure and on other III-V wafer substrates. This process serves in eliminating the need for metal precursor nucleation, decreasing EOT, and lowering border trap density and fixed charged associated with interfacial layers or even direct bonding of oxide to non-silicon semiconductors

This novel technology will be useful during deposition and processing of gate stacks on FinFETs for MOSFETs, the current design used by Intel. The disclosed technology results in surface termination by Si-Cl groups followed by passivation with atomic hydrogen, creating Si-H termination, and surface functionalization. By keeping the Si chemically protected at all times, the layer can be transferred within a typical semiconductor processing tool.

ADVANTAGES

Novel features of this Self-limiting and saturating CVD and ALD technology:

1. Clean the surface and protects against oxidation, Improving the current semiconductor and metal substrate surface preparation and controlled growth methods.

2. Creates a surface which is reactive to ALD precursors (Functionalization).

3. Forms a monolayer which leaves the Fermi level unpinned (Passivation).

RELATED MATERIALS

- Edmonds M, T Kent, R Droopad, E Chagarov, A Kummel. Self-Limiting and Saturating CVD of a Silicon Seed Layer on InGaAs, Materials Research Society Spring meeting, April 2014. URL: http://www.mrs.org/spring-2014-program-bb/# - 04/21/2014

PATENT STATUS

Patent Pending

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OTHER INFORMATION

CATEGORIZED AS

- **Semiconductors**
  - Assembly and Packaging
  - Design and Fabrication
  - Processing and Production

RELATED CASES

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