



# Scalable Parameterized VLSI Architecture for Compressive Sensing Sparse Approximation

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## SUMMARY

Researchers in the UCLA Department of Electrical Engineering have developed a scalable and parameterized VLSI architecture for compressive sensing (CS) sparse approximation, allowing for energy-efficient, cost-effective, and real-time compressive-sampled data processing in wireless/mobile healthcare applications.

## BACKGROUND

Wireless healthcare technology makes medical resources more accessible while also lowering cost, increasing the engagement between patients and doctors and promoting connectivity for improved therapy. One of the key challenges in wireless healthcare is the lack of efficient sensing technology, as the continuous monitoring on health status will inevitably generate large amount of data for transmission/storage/analysis. Today’s digital electronics industry relies on the Nyquist sampling theorem, which requires doubling the size (sample rate) of the signal representation to avoid information loss. However, most natural signals result in a large redundancy in Nyquist-sampled data, necessitating data compression prior to storage or transmission. Recent advances in compressive sensing theory offer an alternative data acquisition framework. However, applying the compressive sensing technology in real-time systems involve solving an optimization problem, which requires iterative-searching algorithms that have high computational complexity and data dependency. Existing software solutions are neither energy-efficient nor cost-effective for the real-time processing of compressively-sampled data, especially when the processing is to be performed on such energy-limited devices.

## INNOVATION

The Markovic Lab in the UCLA Department of Electrical Engineering has created a parameterized and scalable VLSI architecture that can be implemented in programmable logic devices, such as field programmable gate arrays (FPGAs), or system-on-chip (SoC) designs to perform hardware-accelerated sparse approximation—the core processing block for performing the reconstruction or classification of compressive-sampled data. The architecture core supports a floating-point data format with a number of design parameters, providing the necessary flexibility for application-specific customization. By compressing sensor data by a factor of 3, that much power can be saved, extending the battery life of the sensors and offering a significant advantage for wireless and mobile healthcare applications.

## CONTACT

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## INVENTORS

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## OTHER INFORMATION

### KEYWORDS

medical signal processing, signal reconstruction, field programmable gate arrays, FPGA reconstruction, Kintex-7 FPGA, computing resources, configurable processing elements, cost effective data acquisition, hardware acceleration, hardware utilization, orthogonal matching pursuit algorithm, OMP, parallel architecture, real-time signal reconstruction, single precision compressive sensing, signal reconstruction engine, CS reconstruction, wireless healthcare, mobile healthcare, vectors, very large scale integration

### CATEGORIZED AS

- Computer
  - Hardware
- Medical
  - Devices
- Sensors & Instrumentation
  - Medical
- Engineering

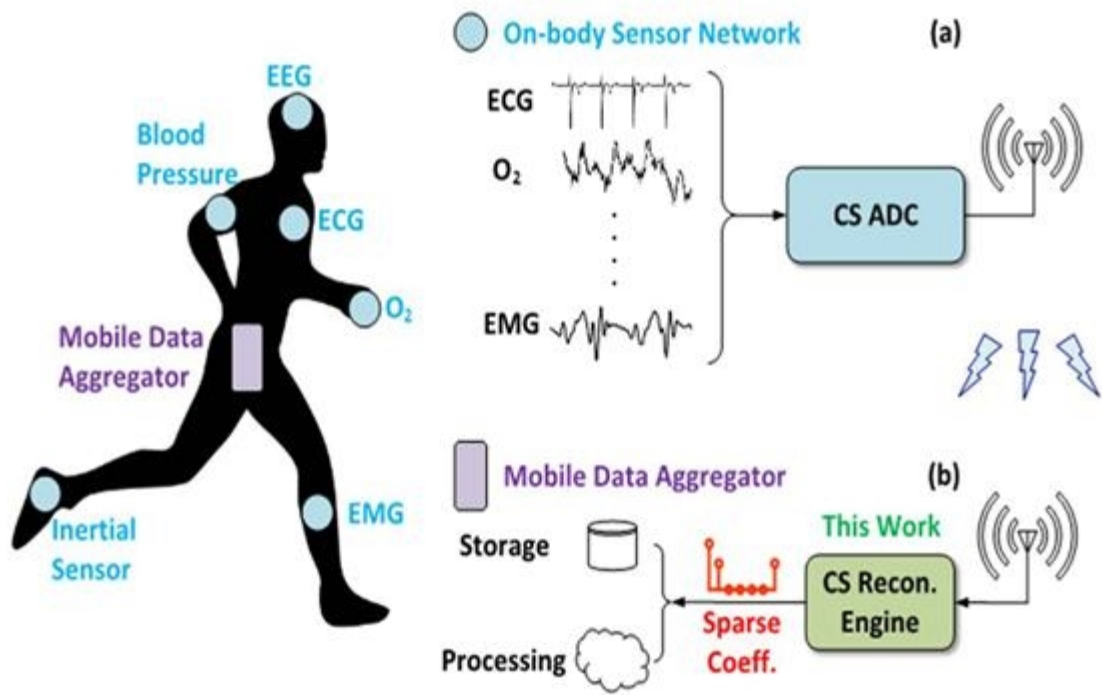


Fig. 1. Illustration of future CS based wireless healthcare systems. (a) CS based on-body sensor network for continuous monitoring. (b) Mobile data aggregator.

APPLICATIONS

Wireless/mobile healthcare:

- Digital signal reconstruction for compressive sampling based data acquisition
- Sparse representation based classification and data separation
- Blind source separation o Signal denoising

ADVANTAGES

- Higher efficiency
- Cost-effective
- Real-time processing

STATE OF DEVELOPMENT

The system has been evaluated on a 28nm Xilinx Kintex-7 FPGA to show the same level of accuracy as the double-precision C program running on an Intel Core i7-4700MQ mobile processor, while providing 47-147 times speed-up and 3-4 orders of magnitude better energy efficiency. A 40nm silicon prototype has also been developed, which can provide real-time sparse signal reconstruction in less than 20mW, as compared to 20W on existing CPU and GPU platforms.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,073,701	09/11/2018	2013-960

RELATED MATERIALS

- Fengbo Ren; Dorrace, R.; Wenyao Xu; Markovic, D., "A single-precision compressive sensing signal reconstruction engine on FPGAs," Field Programmable Logic and Applications (FPL), 2013 23rd International Conference on, vol., no., pp.1,4, 2-4 Sept. 2013 doi: 10.1109/FPL.2013.6645574

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Autonomous Thermoelectric Energy-Harvesting Platform for Biomedical Sensors
- Electrode Agnostic, Supply Variant Stimulation Engine For Implantable Neural Stimulation

- ▶ [A Simple, Area-Efficient Ripple-Rejection Technique for Chopped Bio-Signal Amplifiers](#)
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