Current-Mode Clock Distribution

Tech ID: 23909 / UC Case 2014-341-0

BACKGROUND

Portable electronic devices require long battery lifetimes to meet the longer use times. This can only be obtained by utilizing low-power components, which have become quite critical in system-on-chips (SOCs) because interconnections found in scaled technologies is consuming an increasingly significant amount of power. Researchers have demonstrated that the major consumers of this power are global buses, clock distribution networks (CDNs), and synchronous signals in general.

In addition to power, interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay. Moreover, conventional CDN structures are becoming increasingly difficult for multi-GHz ICs because skew, jitter, and variability are often proportional to large latencies.

Prior to to and in early CMOS technologies, current-mode (CM) logic was the attractive high speed signaling scheme because they were used for long global wires or, more commonly, off chip signals. Standard logic signals, however, have remained in voltage mode (VM) to benefit from low static power of CMOS logic. Researchers at University of California, Santa Cruz, have proposed a scheme that utilizes the power and reliability of CM signaling, yet retain compatibility with low-power CMOS logic.

TECHNOLOGY DESCRIPTION

UCSC researchers' new paradigm for clock distribution uses current, rather than voltage, to distribute a global clock signal with reduced power consumption, making it the first usage in a one-to-many clock distribution network. Inventors created a new high performance current-mode pulsed flip-flop (CMPFF) which enables 45.2% power reduction on average, when compared to traditional voltage mode clock, and is 60% faster on similar silicon real estate. The invention also eliminates the need for complex CM receiver (Rx) circuitry and local VM buffers as in previously proposed CM signaling schemes.

APPLICATIONS

- System-on-chip architecture

ADVANTAGES

- Eliminates the need for complex CM receiver (Rx) circuitry and/or local VM buffers, which reduces power consumption and increases processing on an equivalent silicon area
- Use of current mode rather than voltage mode equates to low production cost

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OTHER INFORMATION

KEYWORDS

Current mode, voltage mode, receiver, CMOS, CM, Clock distribution, Clock distribution networks, CDNs, RX, VM, buffer, CMPFF, multi-GHz ICs, skew, jitter, latencies, System-on-chips, SOCs, transistors, IC, chip design, power, performance, Cat3

CATEGORIZED AS

- **Communications**
  - Other
- **Computer**
  - Hardware
- **Semiconductors**
  - Design and Fabrication

RELATED CASES

2014-341-0, 2011-195-0, 2011-196-0

INTELLECTUAL PROPERTY INFORMATION

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,787,293	10/10/2017	2014-341

RELATED TECHNOLOGIES

- Distributed Energy Conserving LC Resonant Clock Trees
- Mult-Frequency Resonant Clock Meshes

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Methods for Integrated Circuit C4 Ball Placement Considering Package Reliability
- Distributed Energy Conserving LC Resonant Clock Trees
- Mult-Frequency Resonant Clock Meshes

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