Layout Optimization for Time-dependent Dielectric Breakdown Reliability in VLSI

Tech ID: 23223 / UC Case 2013-213-0

BACKGROUND

Time-dependent dielectric breakdown (TDDB) is becoming a critical reliability issue in VLSI design, since the electric field across dielectrics barriers increases as technology scales downward. Moreover, dielectric reliability is aggravated when interconnect spacings vary due to misalignment between via and wire masks. Although dielectric reliability can be mitigated by a larger interconnect pitch, such a guardband leads to significant area overhead.

TECHNOLOGY DESCRIPTION

Given here is a new post-layout optimization approach to mitigate dielectric breakdown and provide design correction prior to manufacture. Experimental results demonstrate an improved interconnect lifetime of as much as 10% following application of this optimization technique. Applying a second signal-aware chip-level TDDB reliability estimation using the stress time of interconnects based on net signals, the chip-level TDDB lifetime is approximately double that obtained by conventional analysis in which interconnects are always assumed to be under electrical stress.

APPLICATIONS

At a 32nm foundry node this layout optimization technique increases chip-level lifetime by 9% to 10%. At a 20nm process and below, the effect will be even more substantial. This improved chip lifetime also means that chips can be operated at a higher supply voltage for a given lifetime if TDDB is the primary limiting factor affecting the allowable supply voltage for a given layout. Further impacts on chip layout such as printability and electromigration should also experience positive improvements.

RELATED MATERIALS

- Post-routing back-end-of-line layout optimization for improved time-dependent dielectric breakdown reliability TB Chan, AB Kahng - SPIE Advanced Lithography, 2013 - 03/29/2013

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,922,161	03/20/2018	2013-213

CONTACT

University of California, San Diego
Office of Innovation and Commercialization
innovation@ucsd.edu
tel: 858.534.5815.

OTHER INFORMATION

CATEGORIZED AS

- **Computer**
  - Hardware
- **Semiconductors**
  - Other

RELATED CASES

2013-213-0