Cognitive Power Management For Memory-Dominated Wireless Communication Systems

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FULL DESCRIPTION

Dynamic voltage frequency scaling (DVFS) techniques is the traditional technique to perform power management where a design tradeoff is performed between power and delay where lower power is attained at the cost of larger delay, typically by running at a lower operating frequency which is set by the weakest performer in the overall system. In a majority of scenarios, the culprit is embedded memories, since they exhibit the highest vulnerability to supply changes as compared to logic. For this reason, when voltage scaling is used, memories are typically treated separately to maintain the margins such that the device will meet timing 100% of the time with the new settings. While, this is true for some applications such as processor memories, there exists a wide variety of applications that are error tolerant by design such as wireless and multimedia devices where the data structures are designed in such a way that there is redundancy inserted in the data stream to compensate for a variety of errors sources. In such systems, DVFS can't trade-off the power saving with the forgiving nature of the system.

University researchers have developed a method for designing power management systems in embedded wireless communication devices. The invention makes use of a derived statistical correlation between memory supply voltage overscaling (VoS) and bit error rate (BER). By using this model to predict memory error rate for a given supply voltage, and knowledge about the channel error rate, the power controller may scale memory supply voltage to introduce the maximum allowable error rate given the fault-tolerance of the data structures used and the transceiver hardware. Thus, the controller may minimize power usage whilst maintaining a BER associated with the desired Quality of Service (QoS).

SUGGESTED USES

Allows wireless transceivers to operate at a lower power level given a certain reliability requirement.

ADVANTAGES

The proposed model enables the system designers to rapidly and accurately design a more efficient power management policy as compared to the traditional power management policies such as DVFS.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,785,220	10/10/2017	2013-374

STATE OF DEVELOPMENT

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OTHER INFORMATION

KEYWORDS

Low power, Wireless communication, Power management, Embedded memories, Fault tolerant, SRAM

CATEGORIZED AS

- **Communications**

The proposed power management has been modeled and simulated at different channel environments for OFDM-based wireless communication systems.

» Wireless

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2013-374-0

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