Low Voltage Transistors

Tech ID: 22947 / UC Case 2006-163-0

BACKGROUND

A critical issue for scaled logic devices is the ability to operate with reduced power supply voltages, both in order to reduce power dissipation and in order to mitigate high electric field related problems. The sub-threshold swing of present metal oxide semiconductor (MOS) devices (at best 60 mV/decade), and the resultant leakage current, is a major impediment to further scaling of power supply voltage.

TECHNOLOGY DESCRIPTION

Engineers from UC San Diego have patented novel transistor designs having a substrate, a structure supported by the substrate including a source, drain, gate, and channel, wherein the source and the channel are made of different materials, and a tunnel junction formed between the source and the channel, whereby the tunnel junction is configured for injecting carriers from the source to the channel. The materials used in the source and the channel are different, and are chosen in order to optimize the tunneling current.

ADVANTAGES

This invention details very low power transistors operated from a 0.3 volt or lower power supply and thresholds as low as 0.1-0.2 volts or lower, and yet do not suffer from large leakage currents in the OFF state. This represents a third of the supply voltage typically utilized by modern logic transistors. Such a significant voltage reduction offers the potential for a great reduction in power consumption. Reduced power consumption is especially beneficial for portable devices that make use of exhaustible or rechargeable power supplies, e.g., batteries. Reduced voltage levels are also beneficial for reducing heat generation and reducing potential interference effects between devices and interconnections between devices.

These new transistors are also able to turn on and off with only a small input voltage. In particular, the invention provides field effect transistors that achieve subthreshold swing lower than 60 mV/decade (which is the typical limit for conventional transistors). At the same time, transistors of the invention are capable of operation at high speeds.

INTELLECTUAL PROPERTY INFO

This technology is protected by US Patent No. 8,148,718 and commercialization rights are available for license.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	8,148,718	04/03/2012	2006-163

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OTHER INFORMATION

CATEGORIZED AS

- **Engineering**
  - Engineering
- **Semiconductors**
  - Design and Fabrication

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