WAFER LEVEL CHIP SCALE PACKAGING TECHNOLOGY FOR INTEGRATED MEMS DEVICES

Tech ID: 22828 / UC Case 2013-032-0

PATENT STATUS

Country	Type	Number	Dated	Case
Japan	Issued Patent	JP6095308B2	02/24/2017	2013-032
United States Of America	Issued Patent	9,284,186	03/15/2016	2013-032

BRIEF DESCRIPTION

Integrated microelectromechanical systems (MEMS) packaging process at the waver-level scale is an important technology for various devices. For example, in a MEMS accelerometer, the central sensor is a free-standing microstructure and it is desirable to protect this sensor. Moreover, it may be necessary for some MEMS devices to encapsulate the microstructures in vacuum environment for applications such as resonant accelerometers or gyroscopes. While many efforts have shown the successful fabrication of encapsulations for MEMS devices, creating an encapsulation membrane spanning several millimeters in width is challenging. One issue relates to the sacrificial layer below the encapsulation membrane which must be etched away with etching holes and these holes must be sealed during the encapsulation process. Another problem pertains to the membrane which must be made strong enough so that it does not collapse on the MEMS structures inside the cavity. In addition to these challenges, processing time for the thin films must be reasonably fast. To address these problems, researchers at UC Berkeley and Toshiba have developed devices and methods for fast, large-scale integration of semiconductor elements, resulting in a chip-scale package having a thin-film hollow-seal structure for MEMS elements.

RELATED MATERIALS

CONTACT

Terri Sale
terri.sale@berkeley.edu
tel: 510-643-4219.

INVENTORS

» Lin, Liwei

OTHER INFORMATION

CATEGORIZED AS

» **Engineering**

» Engineering

» **Semiconductors**

» Design and Fabrication

RELATED CASES

2013-032-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- PMUT for Blood Pressure Monitoring
- Reconfigurable Soft Li-Ion Battery