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Mult-Frequency Resonant Clock Meshes

Tech ID: 22648 / UC Case 2012-872-0

BACKGROUND

VLSI chips contain gates that are synchronized by clock signals. High performance depends on a high clock rate, but if the gates are unable to maintain the same frequency, the chip doesn't perform well. Therefore, to increase performance, the clock signals need to retain multiple frequencies on the same device without using too much power.

The demand for high performance electronic systems has grown, leading to the use of Very Large Scale Integration (VLSI) chips. These chips have been developed to exhibit higher performance and density, and the current technological aspiration is to continue the advancement of these two aspects. These demands, however, require a great deal of power, which in turn creates more heat, leading to circuit failure.

TECHNOLOGY DESCRIPTION

A UC Santa Cruz researcher has invented a solution to this problem by developing a technique to create resonant clock meshes that resonate at multiple frequencies. The invention adds flexibility by allowing clock drivers to drive different frequencies and to save total chip power.

APPLICATIONS

- ▶ Integrated circuit design for VLSI chips

ADVANTAGES

- ▶ Uses multiple resonant frequencies, unlike current techniques using one resonant frequency
- ▶ Significantly enhances functionality and performance in circuits while using less power

INTELLECTUAL PROPERTY INFORMATION

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,143,086	09/22/2015	2012-872

RELATED TECHNOLOGIES

- ▶ [Distributed Energy Conserving LC Resonant Clock Trees](#)
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INVENTORS

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OTHER INFORMATION

KEYWORDS

Very Large Scale Integration chips, VLSI chips, resonant clocks, resonant clock meshes, multi-frequency, integrated circuit, IC, integrated circuit design, resonant frequency, Cat3

CATEGORIZED AS

- ▶ **Computer**
 - ▶ Hardware
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 - ▶ Software
- ▶ **Semiconductors**
 - ▶ Design and Fabrication
 - ▶ Other
 - ▶ Processing and Production
- ▶ **Engineering**
 - ▶ Other

RELATED CASES

2012-872-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- ▶ [Methods for Integrated Circuit C4 Ball Placement Considering Package Reliability](#)
- ▶ [Distributed Energy Conserving LC Resonant Clock Trees](#)
- ▶ [High-Performance Clock Grid Synthesis and Tuning Using Distributed LC Resonant Tanks](#)
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