Vsat Structure for Nonvolatile Memory Device

Tech ID: 22317 / UC Case 2009-453-0

SUMMARY

Provided are a semiconductor device and a method of fabricating the same. At least one mold structure defining at least one first opening is formed on a substrate, wherein the mold structure comprises first mold patterns and second mold patterns that are sequentially and alternatingly stacked. Thereafter, side surfaces of the first mold patterns are selectively etched to form undercut regions between the second mold patterns. Then, a semiconductor layer is formed to cover a surface of the mold structure where the undercut regions are formed, and gate patterns are formed, which fill respective undercut regions where the semiconductor layer is formed.

BACKGROUND

INNOVATION

APPLICATIONS

ADVANTAGES

STATE OF DEVELOPMENT

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	8,664,707	03/04/2014	2009-453
United States Of America	Issued Patent	8,164,134	04/24/2012	2009-453

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Vertical-Stacked-Array-Transistor (VSAT) for Nonvolatile Memory Devices
- Magnetic Memory Bits with Perpendicular Magnetization Switched By Current-Induced Spin-Orbit Torques
- A Read-Disturbance-Free Nonvolatile Content Adressable Memory
- A Self-Organized Critical CMOS Circuit for Computation and Information Processing
- Anti-Ferromagnetic Magneto-Electric Spin-Orbit Read Logic

CONTACT

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OTHER INFORMATION

CATEGORIZED AS

- **Semiconductors**
  - Design and Fabrication

RELATED CASES

2009-453-0

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