Warp Processors: Dynamic Hardware/Software Partitioning

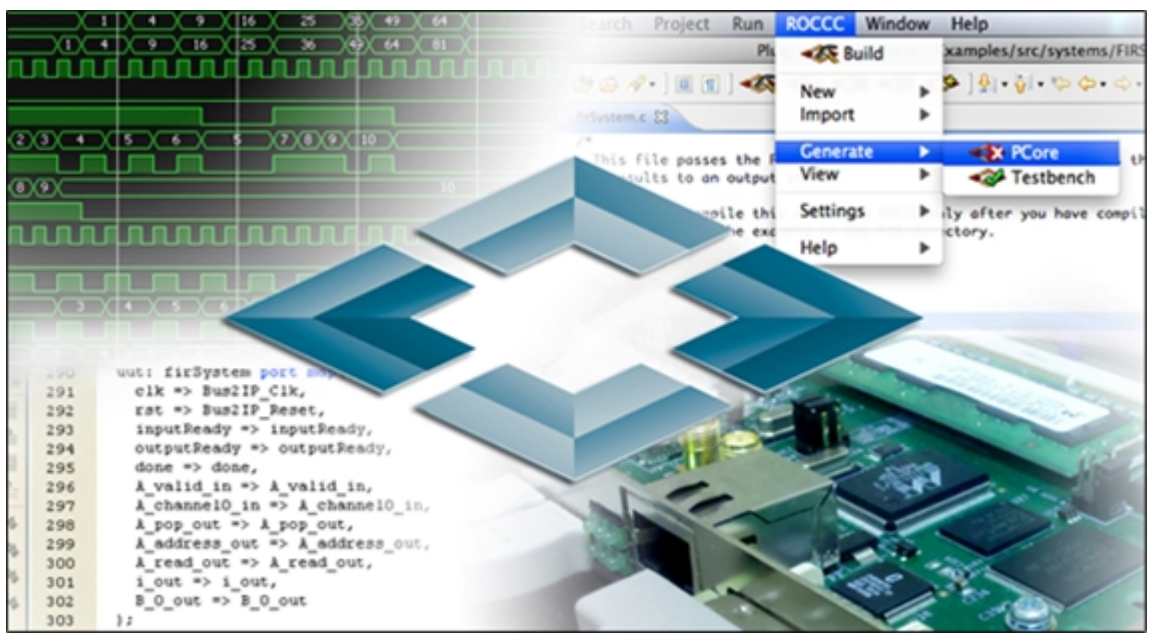
Tech ID: 21788 / UC Case 2004-390-1

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	7,356,672	04/08/2008	2004-390

FULL DESCRIPTION

Traditional microprocessor software bits represent sequential instructions that are executed by a programmable microprocessor. A computation may execute faster on an FPGA than as sequential instructions on a microprocessor because a circuit allows concurrency from the bit to the process level.



Prof. Frank Vahid at UCR has invented a WARP processor, a microprocessor that allows the dynamic and transparent partitioning of an executing software's binary kernels into customized FPGA circuits resulting in 2-100 times speed up over executing on microprocessors.

Prof. Vahid's dynamic approach allows techniques associated with dynamic software optimization to be applied to hardware/software partitioning. The profiler, compiler and synthesis tools are entirely on-chip, so that warp processor partitioning does not require extra designer effort or disruption to standard tool flow.

Prof. Vahid's invention has immense commercial applications as almost any kind of microprocessor-based technology can utilize the benefits of warp processing including video and audio processing, bioinformatics, mainframe computers and even TV's.

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OTHER INFORMATION

KEYWORDS

Microsoftware, Microprocessor, FPGA

Circuits

CATEGORIZED AS

- Computer
  - Software

RELATED CASES

2004-390-1

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Warp processor for dynamic translation of binaries to FPGA circuits

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