High-Performance Clock Grid Synthesis and Tuning Using Distributed LC Resonant Tanks

Tech ID: 21489 / UC Case 2011-196-0

BACKGROUND

Clock signals in digital systems are simultaneously distributed to physical remote locations across an integrated circuit (IC). The clock signal provides a time reference that permits different parts of a circuit to operate in the correct order, thereby producing correct logical operation. Clocking large digital chips with a single high-frequency global clock is becoming an increasingly difficult task. Increasing clock latency in distributing the global clock from a single synchronizing source leads to problems with uncompensated skew, the difference in the clock arrival times between sequentially adjacent registers and jitter, and that which occurs at edges of the clock signal when it fluctuates in time. These problems are primarily due to intra-chip variability and power-supply noise coupling through buffers.

Skew and jitter have traditionally been the dominant concerns in clock design; however, due to increase clock capacitance and frequency in highest-performance microprocessors, dynamic power dissipation is exploding. During every cycle, the entire clock capacitance is charged to the supply voltage, and when this charge is subsequently dumped to ground, all the stored energy is lost as heat.

DESCRIPTION

The new methodologies developed by UCSC researchers undertake the unique challenges of synthesizing the resonant grids in high performance systems. Chip design methodology enhances the usefulness of a resonant clock by achieving additional power savings, along with residual benefits through the automation of current hand tuned processes. The on-chip clock distribution network (CDN) consumes in excess of 35% of total chip power and occasionally as much as 70%. Experimental results, in using this methodology, show CDN power savings as much as 80%. The power savings along with automation enhancement feature are technology improvements which will enable enhanced IC performance.

APPLICATIONS

- Designing VSLI clock distribution networks

ADVANTAGES

- The clock distribution network (CDN) saves as much as 80% power compared to other VLSI chips.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	8,719,748	05/06/2014	2011-196

RELATED TECHNOLOGIES

- Current-Mode Clock Distribution
- Distributed Energy Conserving LC Resonant Clock Trees
- Mult-Frequency Resonant Clock Meshes

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OTHER INFORMATION

KEYWORDS

Clock grid, high-performance, clock distribution network, CDN, digital chip, VLSI, VLSI chips, Cat3

CATEGORIZED AS

- **Computer**
  - Hardware
  - Other
- **Semiconductors**
  - Design and Fabrication
- **Engineering**
  - Other

RELATED CASES

2011-196-0, 2011-195-0, 2014-341-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Methods for Integrated Circuit C4 Ball Placement Considering Package Reliability
- Distributed Energy Conserving LC Resonant Clock Trees
- Mult-Frequency Resonant Clock Meshes
- Current-Mode Clock Distribution

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