

# Distributed Energy Conserving LC Resonant Clock Trees

Tech ID: 21438 / UC Case 2011-195-0

## BACKGROUND

Clock networks in high-performance designs are extremely power hungry. One method to reduce high power consumption is to use distributed LC tanks. By shifting between electrical and magnetic forms at the resonant frequency, these LC tanks conserve energy. However, no physical algorithms for the synthesis of resonant trees have been proposed before now. UC Santa Cruz is the first to present an algorithm to synthesize resonant region clock trees in ASIC’s.

## DESCRIPTION

UC Santa Cruz researchers have developed the first algorithm to achieve significantly reduced power in integrated circuits. UCSC’s highly effective algorithm synthesizes resonant regional clock trees using distributed LC tanks. This resonant technique can be used in both ASIC’s and custom microprocessors, and the algorithm attained a record 41.7% power reduction and an 8.4ps skew reduction. Despite increasing inductor and capacitor area, the algorithm reduces the total buffer area required. Thus, the UCSC algorithm has potential to make clock networks low cost and energy conserving.

## APPLICATIONS

- ▶ Integrated circuits

## ADVANTAGES

- ▶ Over 40% power reduction with a modest 8.4ps skew reduction
- ▶ Reduces the total buffer area required
- ▶ Low cost

## PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,073,93	09/11/2018	2011-195
United States Of America	Issued Patent	8,739,100	05/27/2014	2011-195

## RELATED TECHNOLOGIES

- ▶ [Current-Mode Clock Distribution](#)
- ▶ [Mult-Frequency Resonant Clock Meshes](#)

## CONTACT

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## INVENTORS

- ▶ Guthaus, Matthew R.

## OTHER INFORMATION

### KEYWORDS

algorithm, tanks, Clock, signals,  
digital, systems, frequency, jitter,  
skew, capacitance, power,  
dissipation, chip, savings,, Cat3

### CATEGORIZED AS

- ▶ **Computer**
  - ▶ Other
  - ▶ Software
- ▶ **Semiconductors**
  - ▶ Design and Fabrication
- ▶ **Engineering**
  - ▶ Other

### RELATED CASES

2011-195-0, 2011-196-0, 2014-341-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- ▶ [Methods for Integrated Circuit C4 Ball Placement Considering Package Reliability](#)
- ▶ [Mult-Frequency Resonant Clock Meshes](#)
- ▶ [Current-Mode Clock Distribution](#)

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