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Vertical Nanowire Field-Transistors For Integrated Nanoelectronics

Tech ID: 20728 / UC Case 2006-319-0

BRIEF DESCRIPTION

In the past, the alignment of semiconducting nanowires was achieved primarily through growing nanowires on an epitaxial substrate. However, the ordering and the density of nanowires are difficult to control and patterning electrodes to individual wires is highly impractical. Thus, the applications of highly ordered and high-density vertical nanowires arrays for integrated nanocircuits are greatly constrained.

FULL DESCRIPTION

Researchers at UCI's departments of chemical engineering and materials sciences have solved the inherent problems by growing semiconducting nanowires inside a highly ordered channels of a specific oxide template. Thes nanowires are vertically aligned with an extremely high degree of integration and vertical FETS are then fabricated from these nanowires. Thus, functional digital circuit components such as logic gates and memory elements can be built from these FETs with much higher integration density than current state-of-the-art semiconductor technology.

SUGGESTED USES

Semiconductor, nano fabrication

ADVANTAGES

No need for epitaxial substrate, high ordering and density

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OTHER INFORMATION

CATEGORIZED AS

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