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Efficient Transaction Based Modeling with Cycle Count Accurate at Transaction Boundary (CCATB) Models

Tech ID: 18822 / UC Case 2005-288-0

BACKGROUND

In the past, several modeling abstraction levels were proposed to improve simulation speed and modeling time over detailed cycle accurate (CA) models. The Pin Accurate Bus Cycle Accurate (PA-BCA) modeling abstraction maintained cycle accuracy at every cycle boundary for communication in a system, while capturing all the pins at every component interface. These models were faster to simulate and model than CA models. The Transaction based BCA (T-BCA) modeling abstraction used the concept of transactions from the TLM domain to speed up modeling and simulation time when compared to PA-BCA models. However, both PA-BCA and T-BCA models are still slow to simulate and time consuming to model, for system exploration.

TECHNOLOGY DESCRIPTION

University researchers have developed an abstraction for modeling system designs called CCATB (which stands for Cycle Count Accurate at Transaction Boundaries). Traditionally, systems have been captured with cycle accurate (CA) models for design space exploration which are too time consuming to create and also to simulate. Transaction level models (TLM) are very high abstraction models of the system which are fast to simulate but not accurate for detailed system exploration. The CCATB modeling abstraction maintains observable cycle count accuracy at the boundary of every read or write transaction occurring in the system. Since we are not concerned with maintaining accuracy at every cycle boundary, we can speed up both the simulation speed and the modeling effort. The CCATB modeling abstraction thus allows fast simulation of system models, similar to TLM while maintaining overall cycle accuracy, like in CA models which is essential for accurate system exploration.

APPLICATIONS

The CCATB modeling abstraction has the potential for widespread use among the system design and EDA tool community for creating faster simulation models of systems for rapid exploration of the design.

PATENT STATUS

Country	Туре	Number	Dated	Case
United States Of America	Issued Patent	7,778,815	08/17/2010	2005-288

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OTHER INFORMATION

CATEGORIZED AS

- >> Computer
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