SILICON NANOWIRE VERTICAL SURROUNDING-GATE FIELD EFFECT TRANSISTORS

Tech ID: 17487 / UC Case 2005-051-0

ABSTRACT

As semiconductor devices are scaled into the sub 50 nm regime, short-channel effects and poor subthreshold characteristics begin to be problematic for traditional planar transistors. Novel device geometries with enhanced performance, defined by functional density, energy efficiency, scalability, compatibility with CMOS, are required in order to push toward ever higher packing densities in memories and logic chips with ever increasing energy efficiency. University of California investigators have addressed this challenge by providing vertical silicon nanowire array growth with tight control over size «20 nm), uniformity (± 10%), position (allow addressability), density (106_1012 cm·; scalability), and precise doping. They have demonstrated the first silicon nanowire vertical surrounding gate transistor (Si-NW -SGT). This technology provides the possibility of integrating Si nanowire vertical surrounding gate transistors into arrays and stacks for memory and logic technologies.

In contrast to currently available mentioned, the investigators approach relies on a bottom-up process to produce the precisely defined "channel" (epitaxial silicon nanowire vertical array) of the proposed surrounding gate transistors. This vertical geometry also readily differentiates from the previous work on nanowire transistors, all of which adopt a lateral device geometry. Using directed colloid seeding for VLS-CVD SiNW synthesis provides precise control over nanowire diameter, growth density, and spatial distribution. At the same time, the SiCl4 precursor is highly effective for the growth of vertically aligned, single-crystalline SiNWs. Moreover, these techniques facilitate the direct integration of nanowires into complex systems such as microfluidic devices. The versatility of these growth control methods stems from the use of SiCl4 as the gas phase precursor.

Link to PCT patent application

ADVANTAGES

- «20 nm size
- ± 10% uniformity
- 106-1012 cm density scalability

APPLICATIONS

- sub 50 nm semiconductor devices
- silicon nanowire vertical surrounding gate
- microfluidic devices

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Published Application	20110233512	09/29/2011	2005-051

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OTHER INFORMATION

CATEGORIZED AS

- **Nanotechnology**
  - Electronics

RELATED CASES

2005-051-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- Methods to Produce Ultra-Thin Copper Nanowires for Transparent Conductors

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