

LOW VOLTAGE MEMS FLASH MEMORY

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ABSTRACT

Aggressive scaling of semiconductor memory cells and the dramatic increase in the memory size array demand high density/low cost flash memory. Floating gate flash memory devices are the state-of-the-art in commercial nonvolatile memory, although they suffer from slow programming speed and show a degradation in performance after approximately 105 program/erase cycles. Also, achieving the benchmark 10-year retention time requires an operating voltage of >10V, which in turn requires peripheral supporting circuitry consuming a large portion of the memory chip area. Further, it is questionable whether conventional flash memory devices can be scaled below the 65 nm technology node.

Researchers at the University of California, Berkeley have invented an improved flash memory device with program/erase speeds as fast as a nanosecond at an operating voltage as low as 2V in 0.13 micron technology. Research and modeling to date indicate that the improved device can meet or exceed the 10-year retention time standard, with no performance degradation through 109 program/erase cycles. The memory core density is comparable to state-of-the-art flash memory, and may be aggressively scaled for high density memory chips including solutions below 65 nm. Like conventional flash memory, Berkeley's improved flash memory device is compatible with the current CMOS process flow.

APPLICATIONS

Flash memory

Secure Flash Memory

ADVANTAGES

Program/erase speed as fast as nanoseconds, at low voltage.

Low voltage, high speed, superior retention time, and high density

Memory core density comparable to state-of-the-art flash memory, with significantly reduced peripheral circuitry, to achieve high-density memory chip.

Good scalability, which offers a solution for the 65nm CMOS technology node and beyond.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Published Application	20090121273	05/14/2009	2004-063

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OTHER INFORMATION

KEYWORDS

digital circuits: memory, digital circuits,
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