A Micropower Delta-Sigma Modulator based on a Self-Biased Super Inverter for Neural Recording Systems

Le Wang and Luke Theogarajan

Department of Electrical and Computer Engineering, University of California Santa Barbara
Santa Barbara, CA, USA

Abstract

This paper presents a micropower, supply scalable 2nd order delta-sigma modulator based on a novel self-biased fully differential super inverter for neural recording systems. By employing an enhanced cascode stage and complementary source degeneration, the super inverter achieves 52 dB of differential-mode gain and 42 dB of common-mode rejection ratio, while remaining self-biased at the optimum operating point. The prototype modulator is implemented in a 0.13 µm CMOS process and occupies 0.03 mm^2 chip area. The fabricated IC achieves 66 dB SNR and 62 dB SNDR over the neural signal bandwidth of 8 KHz, while consuming 20 µW from 1.5 V supply. At 1.2 V supply, it achieves 67 dB SNR and 56 dB SNDR, with only 4.8 µW power consumption. The super inverter-based design methodology can be extended to other low power, high speed, and variation tolerant switched-capacitor circuits.

I. Introduction

As the feature size of CMOS technology continues to scale to accommodate the needs of high-performance digital systems, the design of low power, high speed, and variation tolerant analog circuits becomes more challenging due to the voltage headroom reduction and short channel effects. To address these challenges, inverter-based amplifiers have been reported recently [1-2], utilizing the transition region for amplification. The simplicity and versatility of an inverter as an amplifier, even at ultra low supply voltages, make it an attractive solution. However, the DC gain of a push-pull inverter is only 20-30 dB in modern CMOS processes, rendering it unsuitable for high precision analog applications. In addition, the single-ended nature of the inverter necessitates the use of pseudo-differential structures to enhance its noise rejection, which complicates the common-mode feedback design. To improve the inverter's gain performance and attain fully differential operation, a novel self-biased super inverter is proposed and analyzed in this paper. By employing the self-biasing technique, the super inverter can be utilized in the switched-capacitor (SC) circuits for low power, high speed, and variation-tolerant operation. As a prototype, a micro power 2nd order delta-sigma modulator, based on the super inverter, was designed for neural recording systems. Furthermore, a floating sampling scheme was devised to eliminate the need for generating a common-mode reference voltage and enables the incorporation of the super inverter into the modulator.

This paper is organized in the following order. Section II discusses the operation principle of the super inverter. The prototype delta-sigma modulator design and system considerations are described in Section III. Section IV presents the measurement results of the fabricated IC, and Section V concludes the paper.

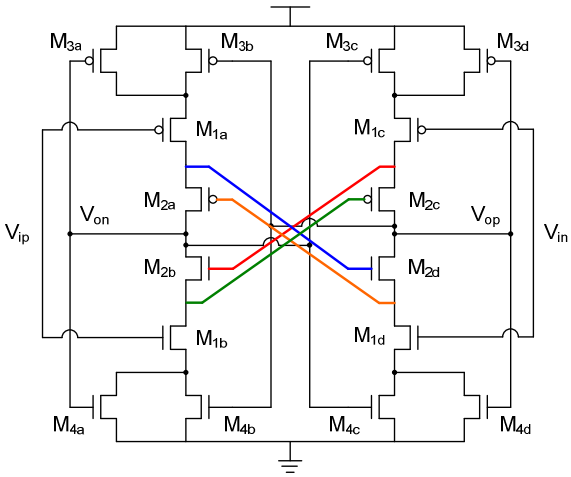

Fig. 1 Circuit schematic of the self-biased super inverter

II. Self-Biased Super Inverter

Fig. 1 shows the circuit schematic of the proposed self-biased super inverter. Compared to a pair of CMOS inverters, the super inverter adds the enhanced cascode stage for differential-mode gain boosting and the complementary source degeneration for common-mode noise rejection and the optimum self-biasing. M_1 serve as the push-pull differential input stages. $M_{3,4}$ form the complementary source degeneration for M_1, with their gate voltages complementarily biased by the differential outputs, V_{op} and V_{on}. From the DC point of view, the internal negative feedback loop not only equalizes the static currents (I_{dc}) through M_1 and $M_{3,4}$ but also corrects any drift in the nominal bias voltages due to process and temperature variations [3]. By biasing $M_{3,4}$ complementarily, the common-mode gain (A_{cm}) of the super inverter is suppressed by the DC loop. For the differential-mode operation, the effects of positive feedback and negative feedback cancel each other, so the differential-mode gain (A_{dm}) is largely unaffected.

The small-signal model of the super inverter, excluding the enhanced cascode stage, is shown in Fig. 2. In the common-mode operation, the internal node voltage V_x tracks the output voltage V_o in the opposite direction, forming a series-shunt negative feedback to stabilize the I_{dc} and suppress the A_{cm}. In the differential-mode operation, the controlling

voltages, V_{op} and V_{on}, are varied differentially and the small-signal currents in the degeneration devices flow into each other. Thus, V_x can be treated as an AC ground for the A_{dm}.

Cross-biased cascode stage M_2 is added to boost the A_{dm}. It operates as follows: in the differential-mode operation, the gate and source voltages of M_2 are varied in opposite directions by the differential input voltages. Assuming the driving capabilities from both the pull-up and pull-down networks are comparable, these node voltages are varied differentially and this effectively doubles the transconductance (g_m) of M_2; in the common-mode operation, the small-signal gate and source voltages of M_2 are level-shifted versions of each other, so the cascode effect mostly vanishes for the A_{cm}. The small-signal model of the super inverter, excluding the complementary source degeneration, is shown in Fig. 3.

First-order formulas for the A_{dm} and A_{cm} are given in the following equations (1) - (5), with V_{cm} representing the nominal common-mode output level. The A_{dm} and A_{cm} formulas are derived based on Fig. 2(a) and Fig. 3(b), respectively, and can accurately predict the gain performance. Simulation shows that the A_{dm} and A_{cm} of the super inverter are 52 dB and 10 dB respectively, while drawing 6 µA static current from 1.5 V supply. At 1.2 V supply, the A_{dm} and A_{cm} of the super inverter are 58 dB and 11 dB respectively, with 1.8 µA static current.

$$Vx \approx \frac{I_{dc}}{2K_n' \frac{W_4}{L_4}(V_o - V_t)} \tag{1}$$

$$\beta = \frac{\partial V_x}{\partial V_o}\Big|_{V_o = V_{cm}} = -\frac{I_{dc}}{2k_n' \frac{W_4}{L_4}(V_{cm} - V_t)^2} \tag{2}$$

$$I_{dc} \approx \frac{K_n'}{2}\frac{W_1}{L_1}\left[V_{cm}(1+\beta) - V_t\right]^2 \tag{3}$$

$$A_{cm} \approx \frac{-g_{m1}r_{o1}}{1-\beta(1+g_{m1}r_{o1})} \tag{4}$$

$$A_{dm} \approx -2g_{m1}r_{o1}g_{m2}r_{o2} \tag{5}$$

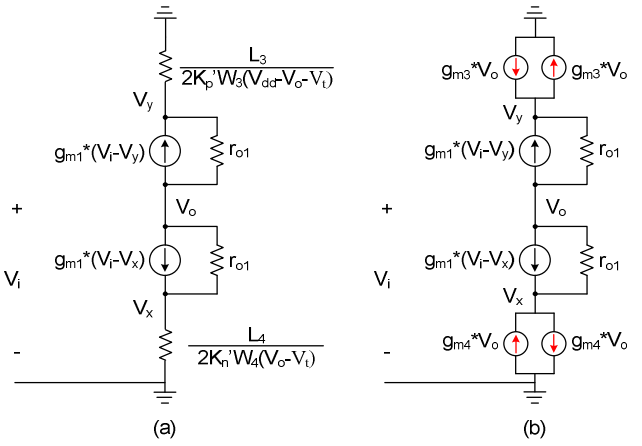

Fig. 2 Simplified small-signal models illustrating the degeneration stages in the super inverter: (a). common-mode; (b). differential-mode

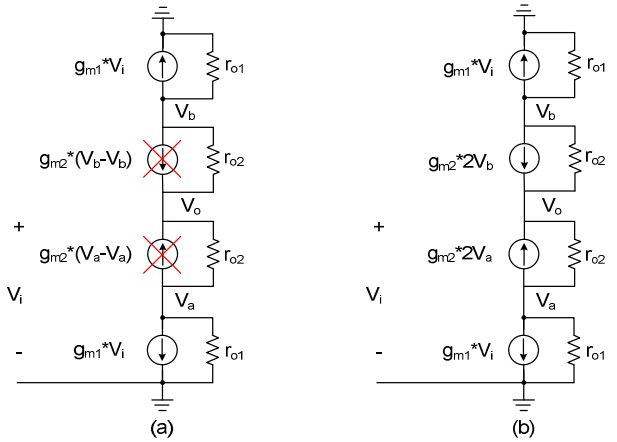

Fig. 3 Simplified small-signal models illustrating the cascode stages in the super inverter: (a). common-mode; (b). differential-mode

III. Delta-Sigma Modulator

To ensure low power operation, a small form factor and relaxed requirements on the analog blocks, a delta-sigma analog-to-digital converter (ADC) is employed in a high-density neural implant IC, as shown in Fig. 4. In contrast to other ADC architectures such as successive approximation (SAR), delta-sigma ADC requires no digital calibration in most implementations, and its resolution can be adapted according to the applications. Due to the internal memory effect, a delta-sigma ADC may be shared by several channels on an interrupt-based manner to optimize the power efficiency and minimize the silicon overhead.

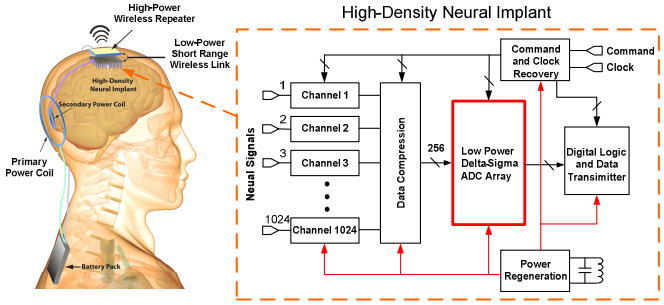

Fig. 4 System diagram of the high-density neural implant VLSI

Fig. 5 shows the super inverter-based 2nd order switched-capacitor delta-sigma modulator. The super inverter replaces the externally-biased operational amplifiers in the SC integrators for micropower operation. Since no external bias network is necessary, this eliminates the on-chip mismatch problems caused by the current mirrors and any noise coupled from the bias network. Moreover, since $M_{3,4}$ operate in the linear region, the super inverter is not slew-rate limited and the switching current can be much greater than the static current, which can be a significant advantage for low power and high speed applications. The delta-sigma modulator uses the Boser-Wooley architecture with two delaying integrators to relax the settling condition. A 1-bit quantizer is selected for high linearity performance. For the same path gain, the two sets of input sampling circuits at the first integrator may be combined to reduce the chip area and the switching noise.

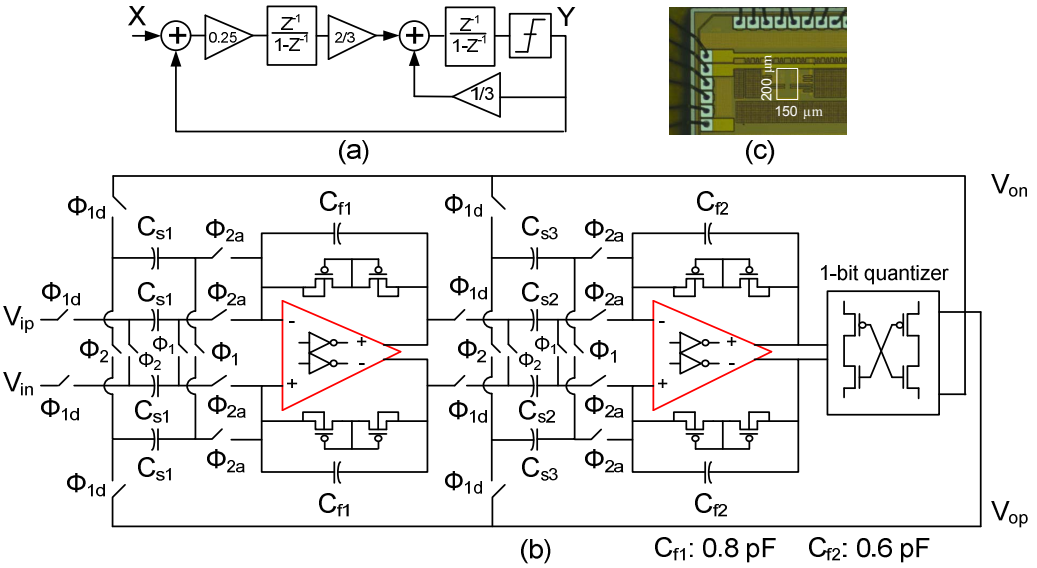

Fig. 5 2nd order delta-sigma modulator: (a) block diagram; (b) circuit schematic (clock generator not shown); (c) chip microphotograph

A switched-capacitor integrator, incorporating the super inverter, is shown in Fig. 6. Floating sampling is devised at both sampling and integration phases to sense differential signals. To illustrate the operation process, assume the two sampling capacitors C_s are perfectly matched and ($V_{ip} = V_c + \Delta V$ and $V_{in} = V_c - \Delta V$). During the sampling phase, the floating potential at the right side of C_s is boot-strapped to V_c and only differential charges $C_s*\Delta V$ are stored onto C_s. Bottom plate sampling is utilized to eliminate signal dependent charge injection by turning off Φ_1 slightly earlier than Φ_{1d}. During the integration phase, the floating potential is level shifted to V_{cm} by turning on Φ_{2a} slightly earlier than Φ_2. Then, Φ_2 switch is closed to transfer the differential charges onto the feedback capacitors C_f. This step is arranged in order to prevent the upsetting of DC operating point of the super inverter. The super inverter has a very narrow input common-mode range, and any difference between its nominal input common-mode voltage and the reference voltage would drift the operating point of the super inverter from the active region. Floating sampling not only mitigates this problem but also eliminates the need for generating a stable reference voltage. Fig. 7 shows the schematic of the clock generator and the associated timing diagram of the non-overlapping clocks. A 2-input NOR gate is utilized to generate the advanced rising edge for Φ_{2a}.

To setup the input DC voltages of the super inverter, two pseudo-resistors connect its input and output ports in a negative feedback, balancing the two common-mode voltages. The pseudo-resistor is formed by two anti-parallel PMOS devices connected in series, which effectively presents a very large resistance (several GΩ) in a small area if the voltage across it is small [4]. The feedback loop in a delta-sigma modulator effectively brings the output levels of the integrators back to its nominal common-mode levels. Therefore, the average voltage across the pseudo-resistor is small, and the condition for the effective resistance is met. The pseudo-resistor also serves as a common-mode feedback (CMFB) device to correct any drift in the input and output common-mode levels of the super inverter over time.

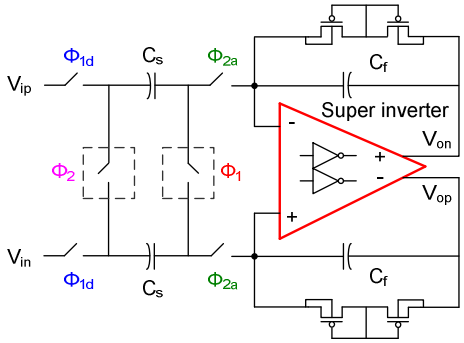

Fig. 6 Switched-capacitor integrator incorporating the super inverter

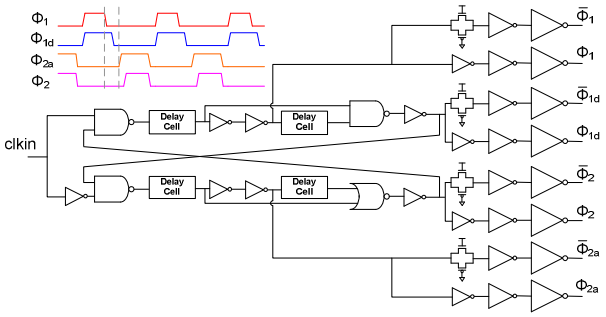

Fig. 7 Non-overlapping clock generator and the timing diagram

IV. Measurement Results

The prototype delta-sigma modulator is implemented in a 0.13 µm CMOS process with eight metal layers and occupies only 0.03 mm^2 chip area, including the clock generator and output buffers. The IC microphotograph is shown in Fig. 5c. A measured output spectrum clocked at 1.6 MHz is shown in Fig. 8. No offset-cancellation mechanism is included in this prototype, and this accounts for the -40 dBFS DC tone in the spectrum. Fig. 9 plots the measured SNR and SNDR over the neural signal bandwidth of 8 KHz versus the input amplitude. The peak SNR and SNDR are 66 dB and 62 dB, respectively. Due to the fully differential nature of the super inverter, the prototype achieves 60 dB power supply rejection ratio (PSRR) as shown in Fig. 10. The measurement results at both 1.5 V and 1.2 V power supplies are summarized in Table I, with the

figure of merit (FOM) defined as in (6). A performance comparison of several recently published SC delta-sigma modulators with this work is given in Table II. Due to the use of the super inverter, this delta-sigma modulator achieves an excellent performance in the power efficiency and PSRR, enabling a high FOM.

$$FOM = \frac{Power}{2 * BW * 2^{(DR-1.76)/6.02}} \quad (6)$$

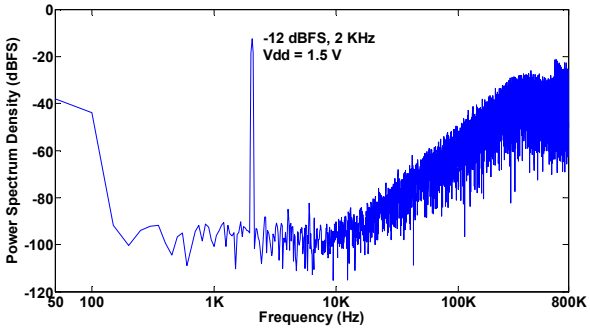

Fig. 8 Measured output spectrum

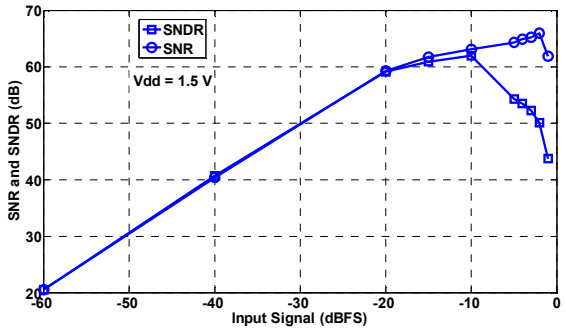

Fig. 9 Measured SNR/SNDR versus input amplitude

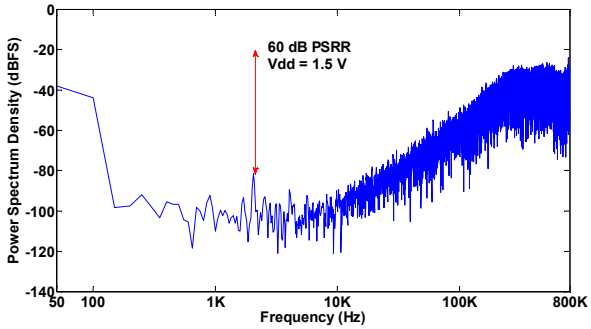

Fig. 10 Measured PSRR with -20 dBFS 2 KHz supply noise while keeping the inputs shorted

TABLE I Summary of measurement results

Supply Voltage	1.5 V	1.2 V
Sampling Frequency	1.6 MHz	
Signal Bandwidth	8 KHz	
Dynamic Range	67 dB	68 dB
Peak SNR @2 KHz	66 dB	67 dB
Peak SNDR @2 KHz	62 dB	56 dB
PSRR	60 dB	
SFDR	70 dB	
Power Consumption in the core*	20 µW	4.8 µW
Total Power Consumption	27 µW	6.5 µW
FOM (pJ/conversion-step)	0.7	0.14
Chip Area/Process	0.03 mm^2/0.13 µm CMOS	

* Excluding power consumption in clock generator and output buffers

Table II Performance comparison

Reference / Technology	BW	Dynamic Range	PSRR	Power	FOM (pJ/step)
[1] */ 0.35 µm	8K Hz	76 dB	37 dB	5.6 µW	0.07
[2] / 65 nm	200K Hz	77 dB	N/A	950 µW	0.41
[5] / 0.18 µm	25K Hz	100 dB	N/A	870 µW	0.21
[6] / 0.18 µm	10K Hz	83 dB	N/A	200 µW	0.86
This work / 0.13 µm	8K Hz	68 dB	60 dB	4.8 µW	0.14

* Modulator-II in [1] is used for comparison

V. Conclusion

This paper presents a novel self-biased fully differential super inverter and its application in a prototype 2nd order switched-capacitor delta-sigma modulator for neural recording systems. By employing the self-biasing technique, the proposed super inverter improves the gain performance and attains fully differential operation. The prototype modulator is implemented in a 0.13 µm CMOS process and the measurement results clearly demonstrate the power efficiency and design flexibility of the super inverter-based topology, and its potential for the design of other low power, high speed, and variation tolerant SC circuits in further scaled processes.

Acknowledgement

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References

[1] Youngchaeol Chae and Gunhee Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits,* vol. 44, no. 2, pp. 458-472, Feb. 2009.

[2] R.H.M. van Veldhoven, R. Rutten, and L.J.Breems, "An inverter-based hybrid ∑Δ modulator," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 492-493, Feb. 2008.

[3] Mel Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165-168, Feb. 1991.

[4] J. Holleman and B. Otis, "A sub-microwatt low-noise amplifier for neural recording," in *Proc. IEEE Engineering in Medicine and Biology Society Conference*, pp. 3930-3933, Aug. 2007.

[5] H. Park, K, Nam, D. Su, K. Vleugels, and B. Wooley, "A 0.7-V 100-dB 870-µW digital audio ∑Δ modulator," in *Symp. VLSI Circuit Dig.*, June 2008, pp. 178-179.

[6] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9V ∑Δ modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 492-493, Feb. 2006.