A Nested Reactive Feedback Power Amplifier for Q-band Operation

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***Abstract*—A power amplifier topology is presented that incorporates a feedback network around the active device that can be tuned for small- and large-signal circuit operation. The PA is fabricated in a 120-nm SiGe BiCMOS process and from 37-47 GHz. The PA achieves a saturated output power of 23 dBm and a peak PAE of 20% at 38 GHz.**

***Index Terms*—Power Amplifier (PA), Silicon-Germanium (SiGe), Power Added Efficiency (PAE)**

I. Introduction

Silicon and Silicon-Germanium (Si/SiGe) circuit processes are poised to challenge the predominance of III-V integrated circuit technologies for power amplifier applications at millimeter-wave bands. High power levels are critical for satellite communication systems at *Q*-band. Monolithic integration of a *Q*-band transmitter requires output power approaching 30 dBm. This paper presents a power amplifier circuit topology implemented in a SiGe process to achieve high output power and high efficiency at *Q*-band.

Two design challenges have arisen for silicon-based mm-wave power amplifiers (PAs). First, the measured efficiency of mm-wave PAs in Si/SiGe processes has remained relatively low (20%). While amplifier classes exist that demonstrate extremely high efficiency at low-frequency, monolithic amplifiers above X-band have not delivered performance at the theoretical efficiency limits. Switching amplifiers - particularly class-E output networks have been investigated using a 120-nm SiGe heterojunction bipolar transistor (HBT) [1][2]. While [1] presents the highest PAE of 20.9%, P_{sat} is limited to 11.5 dBm. It has been suggested that the nonlinear device modeling is limited at high frequency and circuit performance is severely impacted by passive losses and parasitic elements, e.g. emitter or source inductance [3]. Work in CMOS has shown PAE above 20% but typically at lower output power [4] [5] [6].

Secondly, Si/SiGe mm-wave PAs offer limited output power. The 120-nm SiGe HBT has a collector-emitter breakdown voltage (B_{VCEO}) of 1.7 V. This breakdown voltage is much lower than Indium Phosphide or Gallium Nitride but the output power can be increased through the use of on-chip or off-chip power combining. High power SiGe results have shown a saturated output power of 20 dBm but the PAE is limited to 12.7% [7]. To circumvent the power handling limitations, on-chip combining networks - such as the distributed active transformer (DAT) - have been proposed to reach a maximum P_{sat} of 23 dBm but a PAE of 6.4% [8]. These results have indicated trade-offs between power handling and power added efficiency. Power combining approaches suffer from passive losses at high-frequency. Recently, output power and efficiency reaching 20 dBm and 20% has been demonstrated through the use of slow-wave transmission lines which reduce the combiner losses [9].

This work presents a new power amplifier circuit topology which naturally incorporates the parasitic elements of the HBT into a feedback network to achieve both higher output power and efficiency. A nested reactive feedback (NeRF) network is incorporated around an active device to allow higher saturated power levels. A three-stage NeRF amplifier is implemented in 120-nm SiGe BiCMOS and operates from 37-47 GHz with a maximum P_{sat} of 23 dBm and maximum PAE of 20% at 38 GHz.

In Section II, the features of a reactive feedback network are discussed. Section III discusses the small-signal circuit behavior and *S*-parameters to illustrate design constraints on matching and gain. Additionally, the large-signal circuit behavior of a single stage PA is discussed. The circuit implementation in a 120-nm SiGe process is presented in section IV. Section V describes calibration procedures and measurement under different operating conditions.

II. Feedback Networks in Power Amplifiers

To reach high power at millimeter-wave bands, integrated power amplifiers have been most successfully demonstrated based on class-*A* or *AB* operation where the conduction angle of the device is nearly 360^o. A traditional millimeter-wave power amplifier approach is illustrated on the left hand side of Fig. 1. This approach generally consists of an input matching network to improve the power gain and an output matching network to match the load line of the device to a 50 Ω output impedance at the fundamental frequency. To reach high output power, the on-resistance of the device is reduced and larger impedance transformation ratios are required to match to 50 Ω. The finite *Q* of the on-chip impedance transformation - often limited to 20 at millimeter-wave bands - suggests that the output power is also finite for a single stage.

While class-*C* and switching amplifiers, i.e. class-*E* and *F* variants, theoretically achieve higher efficiency, silicon transistors offer limited gain at harmonics of the fundamental. Additionally, the harmonic tuning networks required to generate switching waveforms have low quality factor which limit the efficiency of the power amplifier. Lower conduction angles reduce the gain, subsequently, the efficiency.

An alternative design approach is shown on the right hand side of Fig. 1. In this amplifier, a nested reactive feedback

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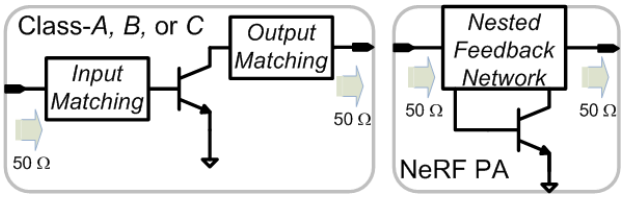

Fig. 1. Comparison of conventional millimeter-wave power amplifier design approach and the proposed nested reactive feedback approach.

(NeRF) network is introduced around the active device to 1) provide the necessary matching conditions at the fundamental frequency, 2) provide impedance transformation from the collector to the output port, 3) control the voltage swing seen across the collector, and 4) mitigate gain compression of the device. The following sections discuss the analysis of each of these features. The concepts presented here are not specific to SiGe HBTs and could also be implemented in CMOS processes.

Feedback is typically avoided in power amplifiers other than to ensure stability since feedback reduces the gain and, hence, the PAE. To illustrate the advantages of the NeRF approach, two PAs are designed for an output power of 23 dBm (200 mW) at 45 GHz. Figure 2 shows the simulated gain and PAE of a single stage class-*A* compared to a single stage NeRF PA based on a 120nm SiGe HBT and lossless passive elements. Most notably, the NeRF PA exhibits reduced gain, however, proper design avoids device compression until much higher output power levels and hence the overall collector efficiency and PAE is much higher than for the class-A amplifier. The active device may be biased with a low conduction angle, e.g. in class-*B* or class-*C*. However, the feedback network linearizes the behavior of the overall power amplifier circuit.

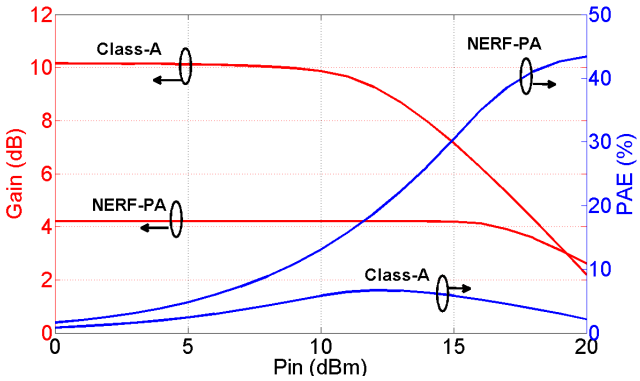

Fig. 2. Simulated gain and PAE of a class-*A* and NeRF PA for 23 dBm of saturated output power based on a 120-nm SiGe HBT. All the passives are ideal.

III. Circuit Analysis

Figure 3 shows a single stage of a NeRF PA and equivalent small signal circuit model. The feedback capacitor across the transconductor is denoted C_μ and incorporates the base-collector capacitance of the device. Input and output capacitors C_i and C_o isolate the device from port one and two. The *LC* network forms a series parallel tank when $g_m = 0$ with an effective capacitance of $C_{eff} = C_i||C_o||C_\mu$ and resonates at $\omega_o = \sqrt{\frac{1}{LC_{eff}}}$. While this resonance suggests an open looking into the network, this section will show that paradoxically the return losses are minimized and the gain is maximized when $g_m > 0$.

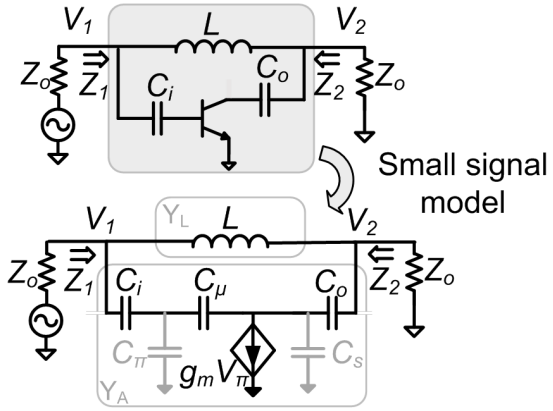

Fig. 3. Single stage of the nested reactive feedback power amplifier and equivalent small-signal circuit model.

A. Derivation of S-parameters

The circuit in Figure 3 consists of two shunt-shunt admittance (*Y*) networks Y_L and Y_A. The first network Y_L is a series inductance;

$$Y_L = \frac{1}{sL}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \tag{1}$$

The second network Y_A is the transconductor with capacitive feedback. The impact of the base-emitter capacitance is initially ignored to illustrate the basic circuit principles, i.e. $C_\pi = C_c = 0$. Later, these capacitances are discussed. For simplification, $C_i = C_o$.

$$Y_A = \begin{bmatrix} \frac{sC_i+g_m}{1+\frac{g_m}{sC_i}+\frac{C_i}{C_\mu||C_i}} & -\frac{s(C_\mu||C_i)}{g_m}\frac{sC_i}{1+\frac{sC_i}{g_m}} \\ -sC_i - \frac{C_i}{C_\mu||C_i}\frac{sC_i+g_m}{1+\frac{g_m}{sC_i}+\frac{C_i}{C_\mu||C_i}} & \frac{sC_i}{1+\frac{sC_i}{g_m}} \end{bmatrix} \tag{2}$$

From feedback theory, the voltage gain is defined as the ratio of feedback and input impedance, $\frac{1/sC_\mu}{1/sC_i}$ when the output port is open. Therefore, the voltage gain is defined by $A_v = \frac{C_i}{C_\mu}$.

The frequency response of a single stage is determined from the shunt-shunt interconnection of (1) and (2). Thus, $Y_S = Y_L + Y_A$:

$$Y_S = \begin{bmatrix} \frac{1}{sL} + \frac{sC_i+g_m}{1+\frac{g_m}{sC_i}+\frac{C_i}{C_\mu}} & \frac{-1}{sL} - \frac{sC_\mu}{g_m}\frac{sC_i}{1+\frac{sC_i}{g_m}} \\ \frac{-1}{sL} - sC_i - \frac{C_i}{C_\mu}\frac{sC_i+g_m}{1+\frac{g_m}{sC_i}+\frac{C_i}{C_\mu}} & \frac{1}{sL} + \frac{sC_i}{1+\frac{sC_i}{g_m}} \end{bmatrix}. \tag{3}$$

For (3), it is assumed C_i is larger than C_μ. In other words, the voltage gain $A_v \gg 1$.

A *Y* to *S*-parameter transformation is applied to (3) [10]. The *S*- parameters are

$$S_{11} = S_{22} = \frac{-\alpha s^3 + (\beta - LC_i)s^2 + (-\gamma + \frac{L}{Z_o})s}{\alpha s^3 + \beta s^2 + \gamma s + 1}, \quad (4a)$$

$$S_{21} = \frac{1 - L\frac{C_i^2}{C_\mu}s^2}{1 + LC_i s^2} . \frac{(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1}{\alpha s^3 + \beta s^2 + \gamma s + 1}, \text{ and} \quad (4b)$$

$$S_{12} = \frac{1}{1 + LC_i s^2} . \frac{(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1}{\alpha s^3 + \beta s^2 + \gamma s + 1}. \quad (4c)$$

where $\alpha = \frac{LC_i^2 Z_o}{2}$, $\beta = \frac{LC_i^2}{2C_{eff} g_m Z_o} + LC_i$ and $\gamma = \frac{C_i^2 Z_o}{2C_{eff}} + \frac{L}{2Z_o}$ are the circuit parameters that determine the poles and zeros of the *S*-parameters.

B. Input and Output Return Loss

The input and output return loss are expressed in (4a). The minimum value of S_{11} and S_{22} occurs when the numerator of (4a) is minimized. This occurs at $\omega_{notch} = \sqrt{\frac{1}{C_{eff}L} - \frac{1}{(C_i Z_o)^2}}$ which is slightly smaller than ω_o. Notably, for high voltage gain ($\frac{C_i}{C_\mu} \gg 1$), ω_{notch} approaches ω_o.

Figure 4 shows the return loss at ω_o for various g_m values. Small g_m suggests that the network is open since β dominates both numerator and denominator in (4a) and the circuit is simplified to a parallel *LC* structure which is open at ω_o. For higher g_m values, the real part of the input (output) impedance drops and the input and output impedance converges to

$$Z_1(\omega_o) = Z_o \left(1 + \frac{j\sqrt{C_{eff}L}}{Z_o(C_i - C_{eff})}\right) \approx Z_o + \frac{j}{\omega_o C_i} \quad \text{for } \frac{C_i}{C_\mu} \gg 1. \quad (5)$$

While the real part of the impedance approaches 50Ω, the imaginary part is inversely proportional to C_i. The input and output matching is improved for larger C_i as shown in Figure 4. The g_m required for return loss better than 10 dB is defined as *critical transconductance* and is approximately

$$g_{m,crit} = \frac{C_i}{C_{eff} Z_o} \approx \frac{C_i}{C_\mu}\frac{1}{Z_o} \quad \text{for } \frac{C_i}{C_\mu} \gg 1. \quad (6)$$

Figure 5 shows the contour plot of S_{11} and S_{22} from (4a) at 45 GHz for $\frac{C_i}{C_\mu}$ and g_m while $C_\mu = 100fF$. L is adjusted properly to keep the tuning frequency at 45 GHz. Increasing both g_m and $\frac{C_i}{C_\mu}$ improves the return loss. For a given $\frac{C_i}{C_\mu} = 2$, any g_m above $g_{m,crit}$ does not substantially improve the return loss.

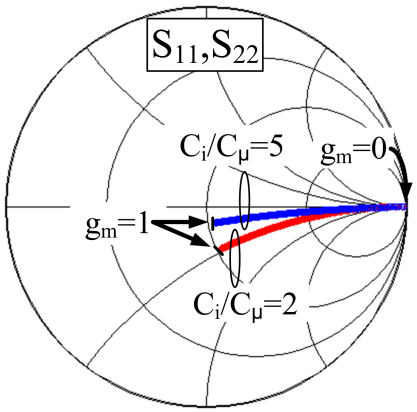

Fig. 4. Effect of g_m on return loss. Higher g_m pushes the real part of the input impedance toward 50 Ω at both input and output ports from (5).

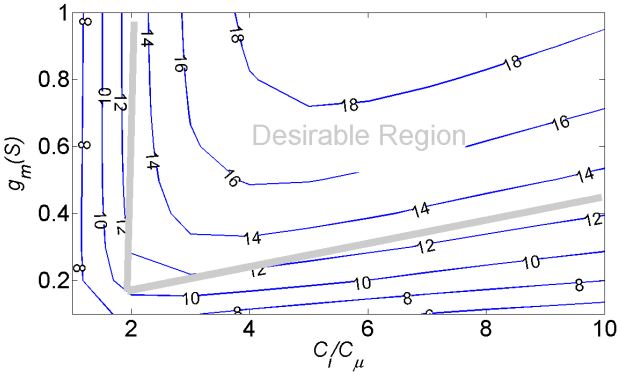

Fig. 5. Contour of return loss of the NeRF PA at 45 GHz for various g_m and $\frac{C_i}{C_\mu}$ ($C_\mu = 100fF$).

C. Gain and Isolation

From (4b), the peak value of S_{21} occurs at $\omega_{peak} = \sqrt{\frac{1}{C_{eff}L} + \frac{1}{(C_i Z_o)^2}}$ when the denominator of (4b) is minimized. While the denominator is common. Consequently, the pole at $\omega = \sqrt{\frac{1}{LC_i}}$ is cancelled with the numerator, $(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1$, of S_{21}.

Now, the S_{11} notch frequency, S_{21} peak frequency and nominal resonant frequency, ω_o, are related through

$$\omega_{notch}^2 + \omega_{peak}^2 = \omega_o^2. \quad (7)$$

For high C_i values, it has been shown that the notch and peak approach ω_o. Figure 6 shows the gain and isolation of a single stage NeRF PA over frequency range of 100 GHz. At the resonant frequency, ω_o, (4b) and (4c) are simplified to

$$S_{21}(\omega_o) = \frac{C_i}{C_\mu}\left(1 + \frac{j}{-C_i Z_o \omega_o + \frac{Z_o}{L\omega_o}}\right) \quad \text{and} \quad (8a)$$

$$S_{12}(\omega_o) = \frac{C_{eff}}{C_i}\left(1 + \frac{j}{-C_i Z_o \omega_o + \frac{Z_o}{L\omega_o}}\right). \quad (8b)$$

Since $A_v = \frac{C_i}{C_\mu}$ and $\frac{C_{eff}}{C_i} \sim (\frac{C_i}{C_\mu})^{-1}$, then the gain is A_v^2 larger than the isolation.

Figure 7 and 8 show the contour of the gain and isolation of a single stage NeRF PA as a function of g_m and $\frac{C_i}{C_\mu}$ at 45GHz. Again, $C_\mu = 100fF$ and L is adjusted properly to maintain a tuning frequency of 45 GHz. Both gain and isolation improve for higher g_m and $\frac{C_i}{C_\mu}$.

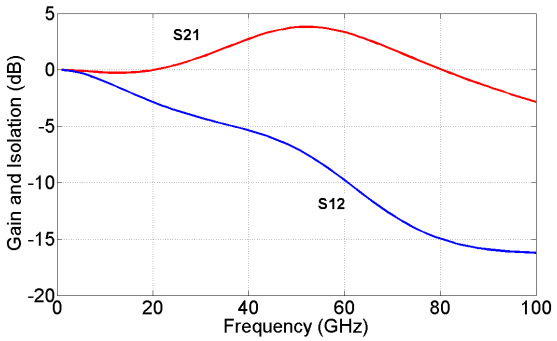

Fig. 6. Gain and isolation of an ideal single stage NeRF PA (gm = 200mS).

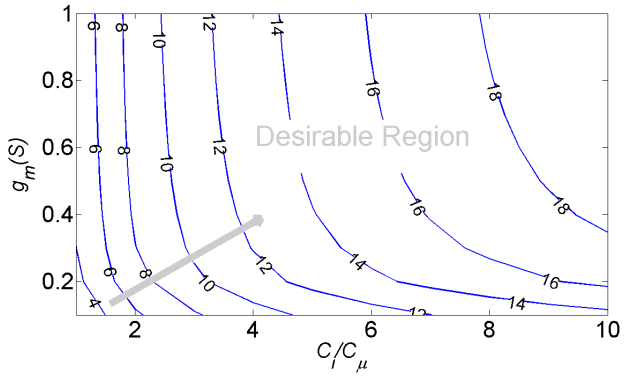

Fig. 7. Contour of gain of a single stage NeRF PA at $f_o = 45GHz$ for various g_m and $\frac{C_i}{C_\mu}$.

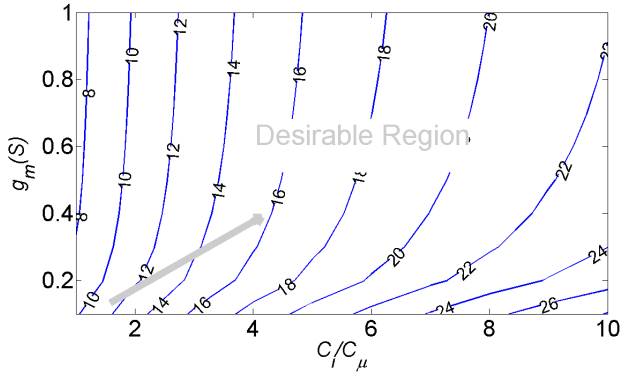

Fig. 8. Contour of isolation of a single stage NeRF PA at $f_o = 45GHz$ for various g_m and $\frac{C_i}{C_\mu}$.

D. Stability

The feedback behavior of the NeRF suggests potential stability concerns. Under certain circuit parameters, the PA is in fact unconditionally stable. The stability of a single stage is determined from the μ-factor;

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|}, \tag{9}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The μ-factor indicates unconditional stability if $\mu > 1$ [11]. From (9), $|S_{12}S_{21}|$ should be less than unity since $S_{21} = \frac{C_i}{C_\mu}$ and $S_{12} \approx \frac{C_{eff}}{C_i}$ at ω_o. Figure 9 shows the stability of a one stage NeRF PA for three different transconductance values across a wide frequency range. For $g_m = 0$, the circuit is a pure passive network which has a constant μ stability factor of 1 over the entire band. The circuit shows unconditional stability to 55 and 60 GHz of bandwidth for a transconductance of 0.1 S and 1 S respectively.

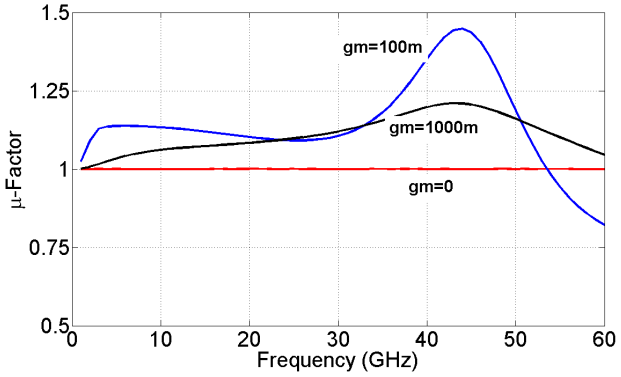

Fig. 9. μ stability factor of a single stage NeRF PA ($Q_{ind} = 20$).

E. Effect of C_π on Small Signal

The previous analysis is based on $C_\pi = C_s = 0$. While ignoring C_s might be valid relative to C_i, C_π is generally significant. Indeed, C_π may be an order of magnitude larger than C_i since g_m is assumed large. Before, matching behavior was identical at the input and output ports, C_π changes the return loss at the input relative to the output.

The notch frequency for input and output return loss is

$$\omega_{notch-S_{11}} = \sqrt{\frac{(\frac{1}{C_i Z_o} - \frac{C_i Z_o}{C_{eff} L})\omega_t}{1 - \frac{C_i}{C_{eff,\pi}} - C_i Z_o \omega_t}} \tag{10a}$$

$$\omega_{notch-S_{22}} = \sqrt{\frac{(\frac{C_{eff,\pi}}{C_i^2 Z_o} - \frac{C_{eff,\pi} Z_o}{C_{eff} L})\omega_t}{1 - \frac{C_{eff,\pi}}{C_i} - C_{eff,\pi} Z_o \omega_t}} \tag{10b}$$

where $\omega_t = \frac{g_m}{C_\pi}$ is the transit frequency of the active device and $C_{eff,\pi} = (C_i + C_\pi)||C_o||C_\mu$. In both (10a) and (10b) cases, the notch frequencies approach ω_{notch} for

$\omega_t \gg \frac{1}{C_{eff,\pi} Z_o}$. For low ω_t, they split apart and complicate matching.

Figure 10 shows the input and output matching of a single stage NeRF PA with the presence of C_π. As f_t increases, both values approach each other such that the return loss and the input and output is indistinguishable.

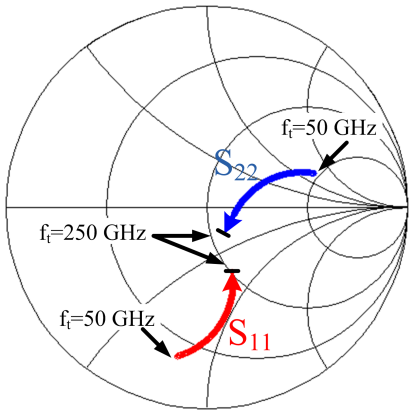

Fig. 10. S_{11} and S_{22} in the presence of C_π. The PA is tuned to 45 GHz for $C_i = 200\ fF$, $C_\mu = 100\ fF$, $L = 250\ pH$ and $g_m = 1\ S$ where $C_\pi = \frac{g_m}{\omega_t}$.

The presence of C_π reduces the gain (S_{21}) since there is voltage division ratio between C_i and C_π. Ignoring C_μ for simplicity, the $V_\pi = V_1 \dfrac{C_i}{C_i + C_\pi}$. This indicates lower gain for higher C_π. This, however, has the advantage of keeping the active device from compression at higher output voltage swings.

F. Large Signal Analysis

Figure 11 shows a simplified large signal model of the proposed amplifier. To consider the nonlinearity, a common emitter amplifier output current is defined as $i_{out} = \sum_{k=1}^{3} g_{mk} v_i^k$ where the g_{mk} is the k^{th} order transconductance. The 1dB compression point voltage can be derived as $V_{1dB} = \sqrt{\frac{0.44}{3}\frac{g_{m1}}{g_{m3}}}$. In the absence of C_i, the base-emitter voltage v_{be} is v_i and even moderate input power levels cause the base to swing below the emitter. For the proposed amplifier, the base-emitter voltage seen through a capacitive divider, i.e. $v_{be} = \frac{C_i}{C_i+C_\pi} v_i$. This effectively modifies the effective transconductance of the circuit to $G_{mk} = g_{mk}(\frac{C_i}{C_i+C_\pi})^k$ [12]. Therefore, the new 1dB compression point voltage is

$$V_{1dB,NeRF} = \sqrt{\frac{0.44}{3}\frac{G_{m1}}{G_{m3}}} = V_{1dB}(1 + \frac{C_\pi}{C_i}). \qquad (11)$$

The 1dB compression point of the circuit increases as C_π does. In fact, as the input voltage increases, more charge will gather in the emitter-base region of the HBT and cause the diffusion capacitance contribution to C_π to increase. The voltage swing across the base-emitter junction is dynamically controlled through this capacitance divider. For smaller values of C_i, the circuit gain drops but the linearity of the device increases.

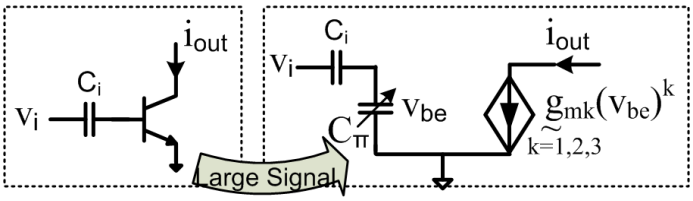

Fig. 11. Simplified large signal model of a common-emitter amplifier with capacitive feedback

The PA near compression is also sensitive to changes in the bias point. The 2nd order nonlinearity of the PA introduces a d.c. component which increases the collector current, forces the device to enter compression, and drops the overall efficiency. [13]. The dynamic behavior of the capacitive divider in the feedack network of the NeRF PA moderates the d.c. tone generation and thereby prevents an increase in the collector current. Figure 12 shows the d.c. component of the collector current for a Class-A and a NeRF power amplifier. Both cases use the same size transistor and identical nominal biasing current. The Ic for each case is the same for lower input power values. As P_{in} increases, the NeRF PA is less effected than Class-A due to the feedback provided by C_i and C_π.

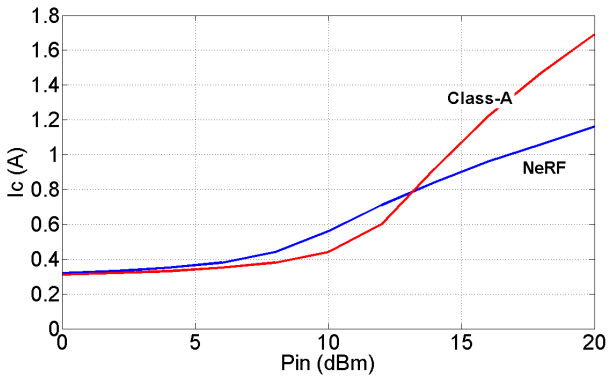

Fig. 12. Dependence of collector current on 2nd order nonlinearity caused by amplifier compression.

The time-domain collector-emitter voltage Vce and collector current Ic of the NeRF PA in section II are plotted in Figure 13 for an input power of 0 and 20 dBm at 45 GHz. Unlike a class-A power amplifier, the Vce and Ic of the NeRF PA is 90 degree phase shifted. This reduces the total power dissipated by the device, making the PA more efficient.

IV. Circuit Design

Figure 14 shows the proposed NeRF power amplifier implemented in a 120-nm SiGe process. It contains three stages with progressive transistor scaling handle higher power levels and prevent each stage from entering compression.

The biasing circuitry of each base has low impedance to improve the breakdown voltage of the device and is capable of both sourcing and sinking current as the device enters breakdown [14]. A 200-Ω resistor provides feedback to prevent

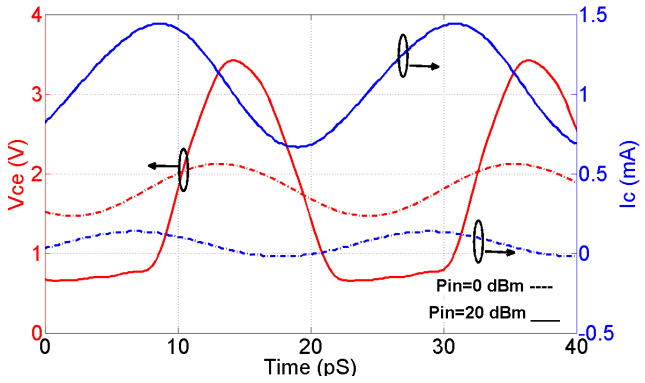

Fig. 13. Vce and Ic of the NeRF PA in section II for P_{in}=0 and 20 dBm.

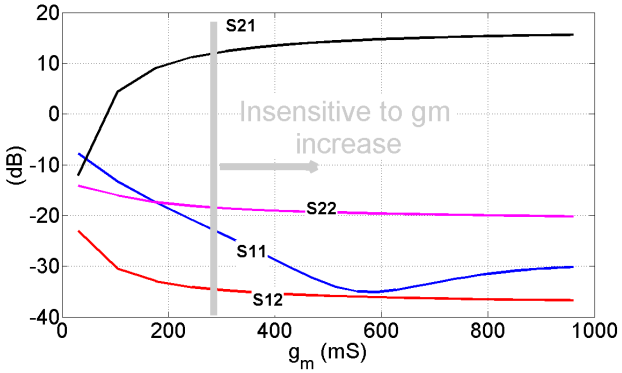

Fig. 15. The S-parameters at 45 GHz for various transconductance show insignificant change for $g_m \geq 300mS$, a value twice than $g_{m,crit}$.

thermal runaway. Quarter-wave transmission lines are used to bias the collector of each device. On-chip 10 pF MIM capacitors provide low impedance at f_o to ground.

For each stage, the tuning inductor is scaled due to the larger base-collector capacitance and hence C_{eff} of each stage to resonate at 45 GHz. The 150 pH series interstage inductor is used to cancel out the capacitive portion of the input impedance for better matching as seen from Figure 4. Table I shows the passive element values and the predicted gain for each stage.

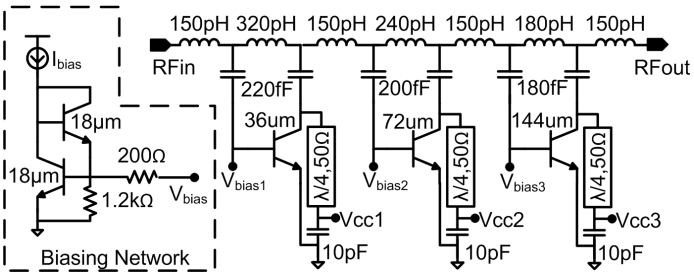

Fig. 14. Schematic of the proposed power amplifier including the biasing network

Stage	$C_i(fF)$	$C_\mu(fF)$	$C_\pi(fF)$	$L(pH)$	Gain(dB)
1	220	40	250	320	8.8
2	200	65	450	240	6.5
3	180	115	850	180	2.3

TABLE I
PASSIVE ELEMENTS OF EACH STAGE WITH PREDICTED GAIN

Figure 15 shows the simulated S-parameter values at 45 GHz as a function of g_m. Notably, beyond a transconductance of 200 mS there is no significant change in the S-parameter values. From (6), the $g_{m,crit}$ is 140 mS and for $g_m \geq g_{m,crit}$, the S-parameters are independent of the transconductance value.

Figure 16 shows the /emphS-parameters of the three stage

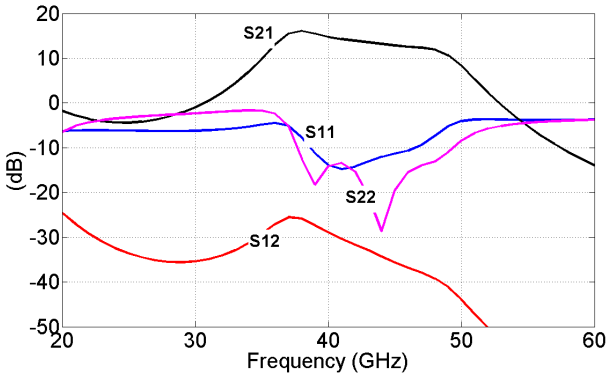

Fig. 16. Simulated S-parameters of the NeRF PA.

NeRF power amplifer. The PA operates from 37 to 47 GHz and has a peak gain of 15 dB at 38 GHz.

To demonstrate the progressive power handling of each stage, the PAE versus input power is plotted Fig. 17. The peak PAE occurs at a higher input power as the signal propagates through subsequent stages.

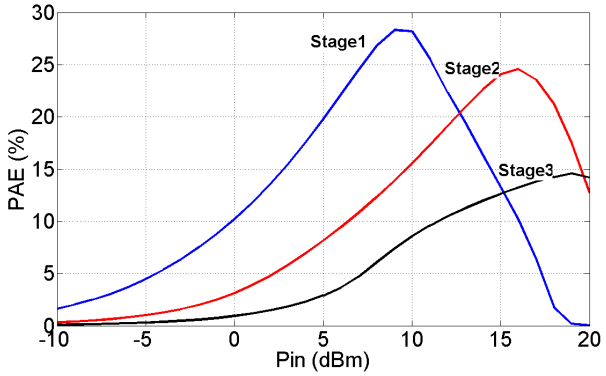

Fig. 17. Scaling of the transistor size and feedback network makes the peak PAE of each stage occur at a higher input power.

Simulated large signal performance of the PA is presented in Figure 18. With a $V_{cc} = 2V$ and $I_{dc} = 4mA$ the PA reaches

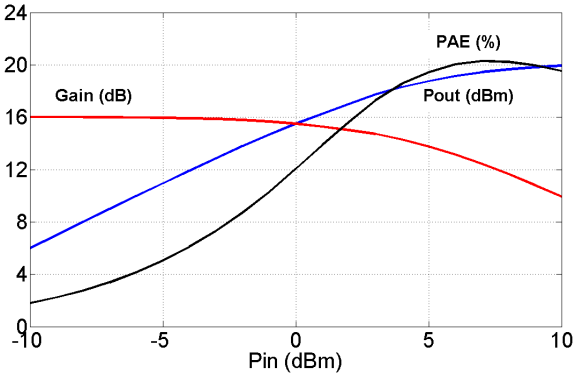

Fig. 18. Simulated large signal performance at 45GHz.

a maximum PAE of 20.1% and Psat of 20 dBm.

V. Measurement Results

The PA is fabricated in a 120-nm SiGe BiCMOS process. Fig. 19 shows the die microphotograph. The circuit measures $1160\mu m$ by $900\mu m$ including pads. The nominal collector current bias for all three stages is 4 mA at 2.4 V collector voltage. The biasing favors class B operation to achieve higher efficiency.

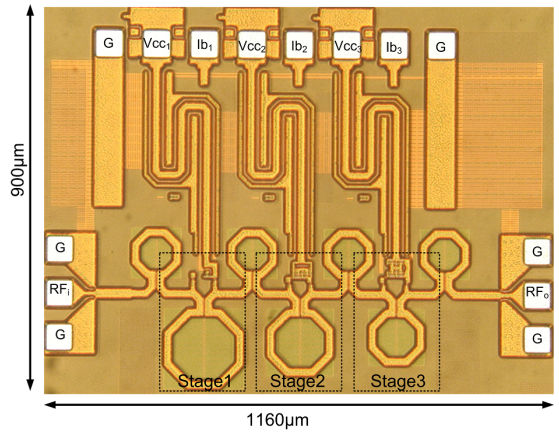

Fig. 19. Die micro photograph of the Q-band NeRF power amplifier

The small signal measurement was performed with an Agilent E8361A two port power network analyzer at room temprature. Figure 20 and 21 show simulated and measured S-parameters of the PA.

Figure 22 shows the large signal measurement setup. Since the Agilent E8257D signal generator (PSG) output power is limited to 14 dBm for frequencies above 30 GHz, an external PA (MARKI A2050) is used to compensate for the cable loss. A 10dB branch coupler (AG 87301) is used to sense the input and output power with an Agilent E4419B power meter. To ensure the power amplifier is not exhibiting any oscillation,

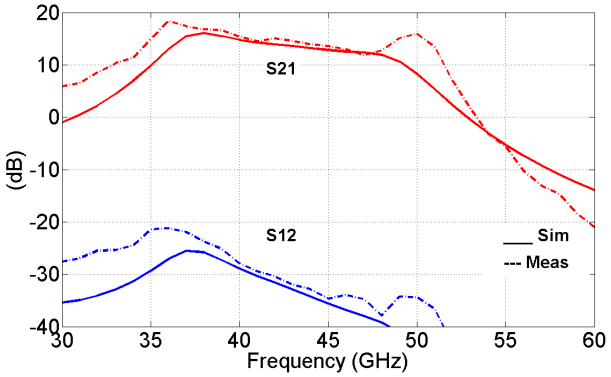

Fig. 20. Measured and simulated gain and isolation of the Q-band NeRF power amplifier

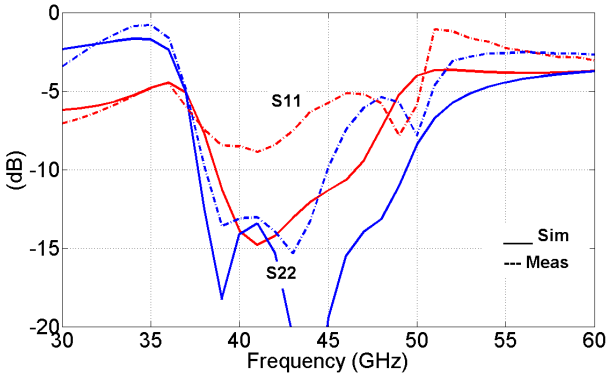

Fig. 21. Measured and simulated return loss of the Q-band NeRF power amplifier

a separate10 dB branch coupler is used at the output node to feed an Agilent E4448A power spectrum analyzer (PSA).

A repeatable calibration procedure of test setup losses is necessary for accurate power and PAE measurement. The following steps were taken to calibrate each component at the input and output. First, channel B of the power meter was connected to point X, right before the input RF probe and $P_{Ch,B} - P_{Ch,A} = 9.95dB$. Thus $P_x = P_{Ch,A} + 9.95dB$. Second, channel B was replaced to the original node as shown in Figure 22 with on-chip thru lines instead of the DUT. This time,$P_{Ch,B} - P_{Ch,A} = 3.72dB$. Since $P_x = P_{Ch,A} + 9.95dB$, the overall loss of two RF probes, two RF pads, the thru line,

Probe Loss	Connector Loss	Cable Loss	Input Offset	Output Offset
0.81 dB	0.1 dB	4.61 dB	9.14 dB	5.42 dB

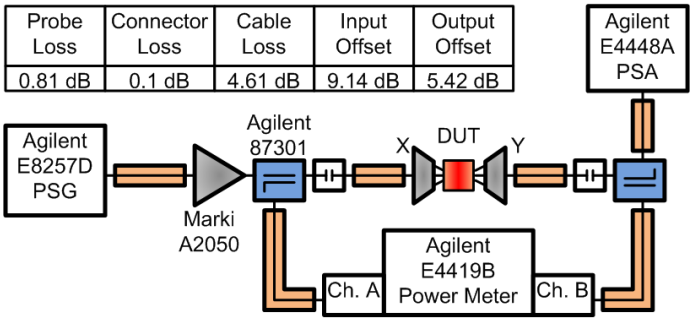

Fig. 22. Large signal measurement setup

and output cables are equal to $6.23dB$. Third, the RF probes, RF pads, and thru line were replaced with a $2.4-mm$ connector. The loss of connector and output cable was measured to be $4.71dB$. Assuming a $0.1-dB$ loss for the $2.4-mm$ connector, the loss of the RF probes and pads, and cables is calculated to be $0.81dB$ and $4.61dB$, respectively. Finally, the input and output power are calculated based on the following formula:

$$\begin{aligned} P_{in} &= P_{Ch,A} + 9.95dB - (RF_{Probe} + RF_{Pad}) \\ &= P_{Ch,A} + 9.14dB \qquad (12) \\ P_{out} &= P_{Ch,B} + (RF_{Probe} + RF_{Pad}) + Loss_{OutputCable} \\ &= P_{Ch,B} + 5.42dB \qquad (13) \end{aligned}$$

The table in Figure 22 shows the loss of each component and the final offset values for the input and output side.

Figure 25 shows the performance of the chip at 38 GHz with a Vcc of 2.4 V and Ibias of 4 mA. The PA achivies a PAE max of 20.05% and a Psat of 21.13dBm at this operating condition. A maximum Psat of 23 dBm was reached for a Vcc of 3 V. Figure 23 and 24 plot the gain, P_{sat} and PAE of the device for the maximum PAE and maximum P_{sat}, respectively. In both cases the peak PAE and peak saturated output power occur at 38 GHz. The peak PAE is shown to be just over 20% for an output power of 19 dBm. The peak output power reaches 23 dBm at a PAE of over 10% and is the best PAE shown at 200 mW in a SiGe process.

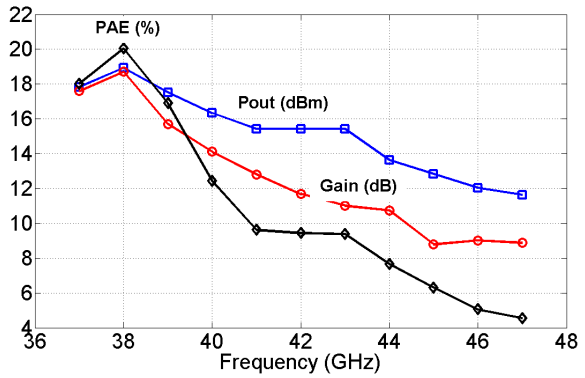

Fig. 23. Maximum PAE biasing condition (Vcc=2.4v, Idc=4mA). The Pout is at the PAE max while the gain is the 1dB compression point gain.

Table II compares this work to prior state-of-the art mm-wave PAs implemented in SiGe or Si CMOS processes. The combination of high output power and high efficiency place this work amongst the best demonstrations at mm-wave bands in Si/SiGe processes.

VI. Conclusion

A new class of power amplifier is presented in 120nm SiGe process. The PA is named Nested Reactive Feedback (NERF) since it is built based on a capasitive feedback at the transconductor and an inductor in the feed farward path. The

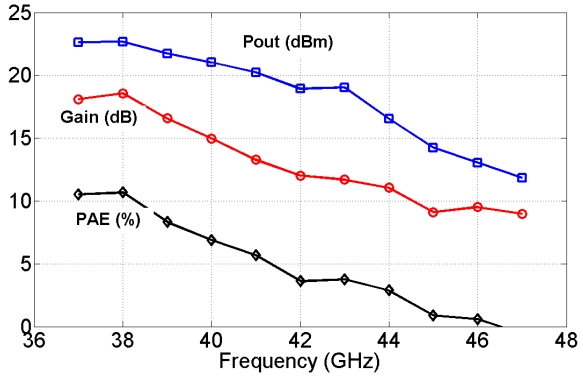

Fig. 24. Maximum Pout biasing condition (Vcc=3v, Idc=4mA). The PAE is at the Pout max while the gain is the 1dB compression point gain.

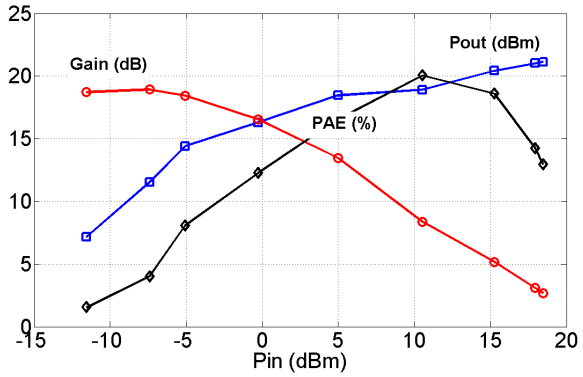

Fig. 25. Large signal performance of the Q-band NERF PA at 38GHz for a Vcc=2.4V. The PA achieves a PAE max of 20.05% and Psat of 21.13dBm

PA has 3 stages and occupies $1160\mu m$ by $900\mu m$ including pads. A maximum PAE of 20.05% and Psat of 23 dBm was achieved for Vcc of 2.4V and 3V respectively at 38 GHz. The PA performs over 10GHz of bandwidth.

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Ref.	Freq. (GHz)	BW (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	Technology
This work	38	10	18.7	21.3	20.0	SiGe 120nm
This work	38	10	18.4	23	10.7	SiGe 120nm
[1]	58	-	4.2	11.5	20.9	SiGe 120nm
[7]	60	-	18	20	12.7	SiGe 120nm
[15]	77	-	17	17.5	12.8	SiGe 120nm
[4]	60	-	9.8	6.7	20.0	CMOS 90nm
[2]	42	8	6	19.4	14.4	SiGe 120nm
[5]	60	6	20.3	18.6	15.1	CMOS 65nm
[8]	60	-	20	23	6.4	SiGe 120nm
[9]	60	10	20	20.5	20	SiGe 120nm

TABLE II
PERFORMANCE COMPARION OF LATEST MM-WAVE PAS

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