Fast Electromigration Analysis For Multi-Segment Interconnects Using Hierarchical Physics-Informed Neural Network

Tech ID: 33148 / UC Case 2023-964-0

PATENT STATUS

Patent Pending

BRIEF DESCRIPTION

Prof. Sheldon Tan and his team have developed a new hierarchical learning-based electro-migration analysis method called HierPINN-EM to solve for multi-segment interconnects in VLSI chips. HierPINN-EM provides much better accuracy, faster training speeds and faster inference speeds compared to current state-of-the-art techniques.

Metrics	HierPINN-EM	EM-Graph	COMSOL
Max RMSE	8.9×10^5 Pa	5.3×10^5 Pa	Ground Truth
Min RMSE	8.4×10^4 Pa	1.9×10^5 Pa	
Mean RMSE	2.8×10^5 Pa	3.6×10^5 Pa	
Mean Error Rate	0.28%	0.36%	
Training Speed	<1min	2hr	N/A
Inference Speed	0.8ms	0.27ms	30min

FULL DESCRIPTION

Background

Electromigration (EM) is the primary reliability killer for copper based interconnects in current and foreseeable nanometer technology nodes. An accurate assessment of aging and reliability for both interconnects and devices during the design process is crucial. Recently, physics-informed neural networks (PINNs) have emerged to replace the traditional numerical discretization with a differentiable deep neural network (DNN) that approximates the solution of the partial differential equation (PDE) as surrogate model. However, plain PINN has limited scalability due to large number of variables and does not work well for large interconnect trees.

Technology

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OTHER INFORMATION

KEYWORDS

chip design, EDA simulation,

electromigration, interconnects, VLSI

CATEGORIZED AS

- Computer
  - Hardware
- Semiconductors
  - Design and Fabrication
  - Testing

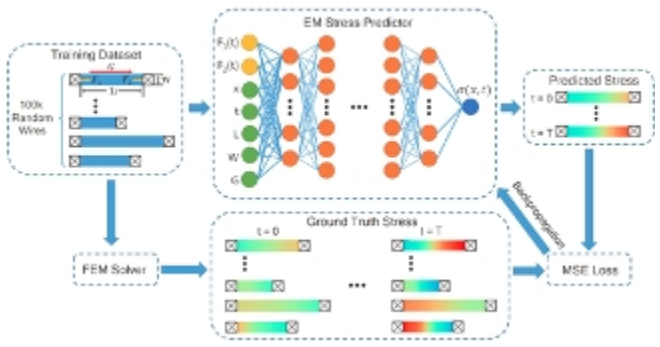
RELATED CASES

2023-964-0

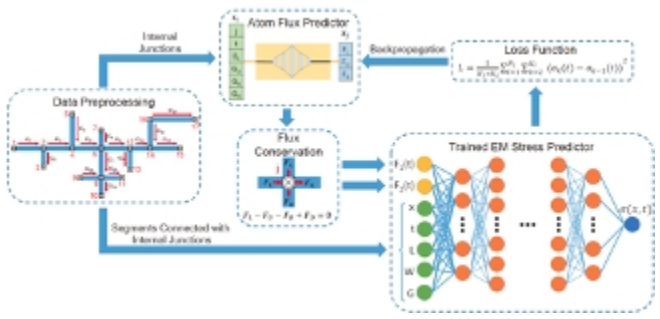
Prof. Sheldon Tan and his team at UCR have developed a new hierarchical learning based EM analysis technique called HierPINN-EM to solve the Korhonen equations for multi-segment interconnects. Instead of solving the interconnect tree as a whole, HierPINN-EM splits the physics laws into two levels and solves the PDE equations step-by-step. The first step of HierPINN-EM is a stress predictor/solver and predicts the EM-induced stress for any location on the wire at a given aging time instant. In the second step, another DNN is employed to output EM stress at the internal junctions.

Images

The two images below show the frameworks for the first and second step.



Framework for the first step



Framework for the second step

ADVANTAGES

Compared with plain PINN, HierPINN-EM achieves much better accuracy (more than 80 times lower root mean square error (RMSE) and much faster training speed (923 times speedup).
HierPINN-EM achieves much faster inference speed.
HierPINN-EM yields better accuracy (19% lower) RMSE with much faster training speed (120 times speedup) compared to EM-Graph.
HierPINN-EM has better result resolution which can be easily controlled at inference time.

SUGGESTED USES

Machine learning EDA simulation for VLSI chip design

INVENTOR INFORMATION

Please visit Prof. Tan's VLSI System and Computation Lab to learn more about their research at UCR.

RELATED MATERIALS

- HierPINN-EM: Fast Learning-Based Electromigration Analysis for Multi-Segment Interconnects Using Hierarchical Physics-informed Neural Network

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