A Low-Cost-Wafer-Level Process For Packaging MEMS 3-D Devices

Tech ID: 28950 / UC Case 2015-807-0

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OTHER INFORMATION

CATEGORIZED AS

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BRIEF DESCRIPTION

A low-cost solution to robust electronic packaging of 3-D MEMS devices using micro-glassblown “bubble-shaped” structures.

FULL DESCRIPTION

Packaging of micro-electromechanical systems (MEMS) and Integrated circuits (IC) is one of the most important and expensive manufacturing steps to bring a product to market. The surrounding package serves as the interface between the circuit electronic elements and the surrounding atmosphere and climate. Depending on the circuit needs, often the MEMS or IC elements will need to be hermetically sealed and protected to ensure proper circuit performance. Current manufacturing methods for proper electronic packaging are limited to size and form factor of MEMS or IC circuits. A new packaging technique is needed to accommodate the varying sizes and 3-D form factors of current day MEMS and IC devices.

Researchers at the University of California, Irvine, have developed low-cost, and scalable means of hermetically sealing 3-D electronic circuits. Through the development of glass micro-bubbles with sealing rings, researchers have achieved vacuum level packaging for a varying size of 3-D electronic circuits. Micro-bubbles glass chambers are manufactured through a pressure induced plastic deformation of a thin layer of borosilicate glass. Variable height of the glass blown bubble structure can be controlled by varying the size of the air trapped cavities underneath the initial deposited layer borosilicate glass. By using this newly developed glass bubble sealing electronic packing process, the mass manufacturing cost associated with packaging non-uniform 3-D electronic circuits form factors can be reduced.

SUGGESTED USES

Hermetically sealing 3-D MEMS devices during the electronic packaging phase of device commercialization

ADVANTAGES

- Reducing the cost associated with developing custom electronic packaging of 3-D MEMS devices
- Scalable electronic packaging methodology. The method is not limited by size or form factor of 3-D MEMS devices.

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,167,190	01/01/2019	2015-807

STATE OF DEVELOPMENT

A batch wafer-level and chip-level packaging process were developed and characterized for 3-D MEMS devices.

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