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Frequency Discriminator-based Phase Noise Filter (PNF) for Ultra-Clean LO/Clock

Tech ID: 25946 / UC Case 2014-999-0

ABSTRACT

Researchers at the University of California, Davis have developed a phase noise filter (PNF) circuit with wide bandwidth and high sensitivity.

FULL DESCRIPTION

Phase noise limits the performance of many microsystems. Phase noise within clocks or local oscillators interferes with the bit-error-rate of digital systems and the resolution of analog-digital/digital-analog converters. It also interferes with the signal-to-noise ratio of radio-frequency systems. This interference compromises between phase noise performance and wide bandwidth and flexibility.

Researchers at the University of California, Davis have developed a passive delay line frequency discriminator and delay line frequency discriminator and phase detector/charge pump-based phase noise filter (PNF) circuit that achieves wide bandwidth and high sensitivity. The PNF circuit has reliable integration capabilities at 10 GHz due to its insensitivity to amplitude and coupling noise. The circuit also offers a high potential solution for ultra-sensitive, high-reliability, and on-chip phase noise measurements. The phase noise filter has already been used in a proof-of-concept demonstration to suppress clock phase noise >15 dB.

APPLICATIONS

- Communications
- Imaging
- Sensors
- Radar

FEATURES/BENEFITS

- Compact
- Wide bandwidth
- Great sensitivity
- Integrability with complex multi-mode and multi-standard systems
- Suitable for integration
- Insensitivity to amplitude and coupling noises

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	10,075,145	09/11/2018	2014-999
United States Of America	Issued Patent	9,667,219	05/30/2017	2014-999

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OTHER INFORMATION

KEYWORDS

phase noise filter, phase
detector, phase noise, PNF
circuit, frequency
discriminator

CATEGORIZED AS

- **Engineering**
 - Engineering
 - Other
- **Semiconductors**
 - Design and Fabrication
 - Other

RELATED CASES

2014-999-0

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